# REVIEW

of the

TRICAL COMMUNICATION LABORATORY

ON TELEGRAPH AND TELEPHONE PUBLIC CORPORATION

Former Reports of the Electrical Communication Laboratory
Nippon Telegraph and Telephone Public Corporation
from Vol.1, No.1, Sept. 1953 to Vol. 7, No. 12, Dec. 1959

*Published Bimonthly by*
E ELECTRICAL COMMUNICATION LABORATORY
PPON TELEGRAPH AND TELEPHONE PUBLIC CORPORATION
1551, Kitizyôzi, Musasino-si, Tôkyô, Japan

VOLUME 8
NUMBERS 3-4

March-April
1960

# Review of the Electrical Communication Laboratory

## EDITORIAL COMMITTEE

Susumu OKAMURA *Chairman*

Tadasu FUKAMI
Giichi ITO
Hideo KAWASAKI
Yukio NAKAMURA
Tatsuya SHIMBORI
Takuzo SHINDO
Toyotaro SHIRAMATSU
Takakichi UZAWA
Ginsaku YASAKI

Koji MAEDA
Nobukazu NIIZEKI
Osamu TUKIZI

## EDITORIAL STAFF

Susumu HIRANO *Editor*
Tutomu SAITO *Assistant Editor*
Sôsuke KOIKE 〃

The Review of the Electrical Communication Laboratory is published 6 times a year (bimonthly) by The Electrical Communication Laboratory, Nippon Telegraph Telephone Public Corporation, 1551, Kitizyôzi, Musasino-si, Tôkyô, Japan. Telephone: Tôkyô-(391) 2261 or 2271.

All rights of republication, including translation into foreign languages, are reserved by The Electrical Communication Laboratory, NTT.

Subscriptions are accepted at ¥1,200 per year. Single copie ¥300 each. Foreign postage is ¥300 per year or ¥50 per copy. Remittance should be made in check payable to the Electrical Communication Laboratory and mail to the Director.

Printed by Aoyama Pinting Co., Tokyo Japan

REVIEW
of the
ELECTRICAL COMMUNICATION LABORATORY

NIPPON TELEGRAPH AND TELEPHONE PUBLIC CORPORATION

Volume 8, Numbers 3-4 March-April 1960

518. 5:681. 142. 004

# A Computer Program to Find Boolean Functions Representable by a Single Logical Element Based on a Majority Decision Principle*

*Saburo MUROGA*†

*Logical elements based on a majority decision principle, like the neurons in living organisms, have been realized recently with parametrons or magnetic cores and are increasing in importance as components for use in constructing computers. An advantage of such elements is that even a single element of this sort can perform fairly complex operations. In this paper a program for the parametron computer "MUSASINO-1" which is to search for Boolean functions representable by a single element and their structures is described. The results will be useful in designing networks with such elements.*

## Introduction

When we make programs properly, electronic digital computers can be useful for non-numerical problems but, at least for the moment, there is no systematic procedure in programming such problems. A program in this paper is of such a nature as to solve a logical problem. The parametron computer MUSASINO-1 in a fixed-point system provides several instructions of logical operations, so it may be suitable for this kind of problems. As a matter of fact, almost half of the problems operated on by this computer since March 1957 are of this kind.

This paper will deal with a problem which occurred in the logic of the elements which perform logical operations in electronic digital computers or in the neurons of human organisms. These elements, which have characteristics different from those of conventional logical elements used in digital computers, depend upon a principle of majority decision. Their major advantage is that even a single element of this sort can perform a fairly complex logical operation. Though higher speed digital computers will be required in the future, possibly we must meet this requirement by paralleling a number of logical elements since the switching speed of any element is physically limited. In this sense, the elements working on the majority decision principle may be important, because this principle is quite simple and a digital network can be constructed with fewer elements and with higher speed.

The theories of the elements and their circuits will be discussed elsewhere. Here, a program to search for function representable by a single element of this sort is described. The program which was actually constructed with instructions for the parametron computer MUSASINO-1, is of a combinatorial type, though an algorithm to construct and element from a given Boolean function will be described elsewhere. The former approach was tried to check the latter approach from an entirely different viewpoint.

---

* MS in Japanese received by the Electrical Communication Laboratory, April 17, 1959. Originally published in the *Electrical Communication Laboratory Technical Journal*, Vol. 8, No. 6, pp. 614–622, 1959.

† Electronics Research Section.

### 1. Mathematical Representation of a Function Represented by a Single Majority Element

Variables $x_1, x_2, \cdots\cdots, x_p$ are coupled to a single majority decision element as inputs, where values of these variables take a value of either 0 or 1 and where $p=2\alpha+1$. If the relative amplitudes of the couplings of these inputs are uniformly one, the majority decision principle states that an output of the element is one or zero, respectively, according to whether the number of ones or the number of zeros is in the majority in the input values. Such a function can be represented as a logical sum of all logical products of $(\alpha+1)$ variables, as follows

$$f(x_1, \cdots\cdots\cdots, x_p)=x_1 \cdot x^2 \cdots\cdots\cdots x_\alpha \cdot x_\alpha+1+x_1 \cdot x_2 \cdots$$

$$\cdots\cdots x_\alpha \cdot x_\alpha+2+\cdots\cdots\cdots+x_{p-2} \cdots\cdots\cdots x_p. \qquad (1)$$

where "+" and "•" indicate the logical sum and product, respectively.

Though the relative coupling amplitudes of the inputs were assumed one in the above case, these amplitudes are not necessarily so and can be any positive integers which will henceforth be called "coupling numbers," If a constant input which takes a permanent value of either zero or one is coupled the element besides in the variable inputs, the number of function representable by a single element is multiplied and expressions for these functions are easily obtained from Equation (1). For example, if a coupling number of the variable $x_m$ is 2, an expression is obtained by putting $x_m=x_{m+1}$ in (1) and if a constant input of zero is to be coupled with a coupling number 3, its expression is obtained by setting $x_k=x_{k+1}=x_{k+2}=0$. Of course, the number of the variable will be smaller than $p$.

Let the coupling numbers of the variable inputs $x_1, \cdots\cdots\cdots, x_k$ and a constant input be $\omega_1, \cdots\cdots\cdots, \omega_k$ and $\omega_c$, respectively. The total sum of the coupling numbers of the inputs,

$$K=\omega_1+\cdots\cdots\cdots+\omega_k+\omega_c, \qquad (2)$$

should always be odd and will be henceforth called the total coupling number. The threshold of the element is defined as

$$T=1/2[(\omega_1+\cdots\cdots\cdots+\omega_k)+1\pm\omega_c], \qquad (3)$$

where − and + in the bracket should be used according to whether the constant input is 1 or 0. As can easily be seen, the output value is 1 only if a sum of coupling numbers of variables taking one is equal to or over the threshold.

In Fig. 1, a simple example is shown. Variables $x_1$, $x_2$, $x_3$, $x_4$, and a constant 0 are coupled to a single majority element with coupling numbers 1, 1, 2, 2, and 1, respectively. Then its threshold is four and it expresses the function:

$$x_1x_2x_3+x_1x_2x_4+x_3x_4. \qquad (4)$$

In this figure, a circle represents the element and a constant input 1 or 0 is shown by + or − with its coupling number, inside the circle.

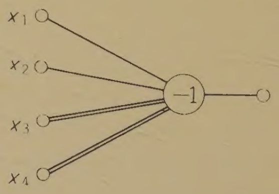


**Fig. 1**—An example of a majority decision element.

## 2. Restriction on Expressions of Functions

Though even a single element with variable inputs can represent various functions, it can not express all possible functions of variables. First we will show what terms an expression of a representable function contains. Let $x_\alpha, x_\beta, \cdots\cdots\cdots, x_\varepsilon$ be a set of variables where the sum of their coupling numbers is equal to or over the threshold and where if any one of the variables is eliminated the sum of the remaining coupling numbers will be less than the threshold. A function for the element is representable by a logical sum of all logical products $x_\alpha x_\beta \cdots\cdots\cdots x_\varepsilon$ of such variables. From the deletion law of the Boolean Algebra, products which include the above products as factors can be deleted from the function.

The following types of restrictions on expressions of functions have been known. That is, functions which include both negatives and affirmatives of the same variables under any Boolean equivalence transformations and functions which do not include a cross product of any two terms included, can not be represented. For example, a function $\bar{x}_1x_2+x_1\bar{x}_3$ can not be represented by a single majority element. For function which can be represented by a single majority element, the following theorem, the proof of which is given elsewhere will be presented. Theorem; A function which a single majority decision element can represent is expressed by a polynomial with logical sums and logical products but without negatives. And for any two terms equal to or higher than the second degree in this polynomial function, if existing, at least one of the cross terms where a variable in each term is replaced by another variable included in the other but not in this term, must exist in the function expression or be deleted by another term.

For example, the function $x_1x_2+x_3x_4$, does not include any of the cross terms, $x_1x_3$, $x_1x_4$, $x_2x_3$, and $x_2x_3$, and therefore can not be represented by a single element.

## 3. A Program to Find Expressions of Functions Representable by a Single Majority Decision Element

If all the coupling numbers of the inputs are given, an expression for a function representable by a single element can be easily obtained, as described in the previous section. However since the procedure is unwieldy when a large number of inputs is considered, the parametron digital computer MUSASINO-1 was used for the task.

For covenience, the threshold $T$ and the total sum of the coupling numbers of the variables $V$ are taken as parameters for the $E$th element. Conversely if these $T$ and $V=\omega_1+\cdots\cdots\cdots+\omega_k$ are given, a polarity and a coupling number of its constant input can be specified according to (2) and (3), but a coupling number of each variable can not be specified. Therefore if all possible combinations of values of $\omega_1, \cdots\cdots\cdots, \omega_k$ are considered for a given $V=\omega_1\cdots\cdots\cdots+\omega_k$ (where $1\leqq k\leqq V$), an expression of a function for each combination will be obtained. For example, if $V=4$, we have five different combinations of $\omega_1$, $\omega_2$, $\omega_3$, and $\omega_4$, as 4,0,0,0; 3,1,0,0; 2,1,1,0 and 1,1,1,1. Then if $T$ is given for each combination, $\omega_c$ is defined and a function expression for each is obtained. We must check all possible partitions of $V$.

### (a) Structure of the Program

A flow chart for the program is shown in Fig. 2. In block B1, by a subroutine which will be described in (b), a partition of a given positive integer $V$ is generated and according to its result coupling numbers $\omega_1, \cdots\cdots\cdots, \omega_k$ are assigned to variables $x_1, \cdots\cdots\cdots, x_k$. Then in B2 and B3, those combinations of binary values of input variables having coupling numbers equal to or over the threshold must be found. Whenever such a combination of variable values is found, the control of the program goes to B4 from B3, checking out whether a new combination is included in a table of already acquired combinations stored in the memory

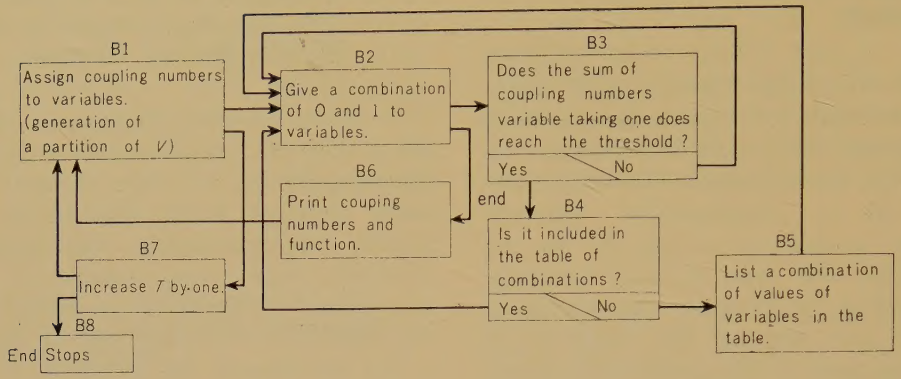

B1
Assign coupling numbers to variables. (generation of V) a partition of V)
B2
Give a combination of 0 and 1 to variables.
B3
Does the sum of coupling numbers variable taking one does reach the threshold ?
Yes
No
B6
Print couping numbers and function.
end
B4
Is it included in the table of combinations ?
Yes
No
B5
List a combination of values of variables in the table.
B7
Increase T by one.
B8
End
Stops

Fig. 2—Flow chart of a program.

of the computer. If it is not, the block B5 performs a role to put it into the table.

When all possible combinations of 0 and 1 are given to the variables, all terms which are to appear in the function are listed in the table. Then B6 printing the coupling numbers of the variables and the function from the table. For example, if $\omega_1=\omega_2=2$, $\omega_3=\omega_4=\omega_5=1$, $T=2$, its function is $x_1+x_2+x_2x_4+x_3+x_5+x_4x_5$ but actually for convenience of printing, coupling numbers will be printed as

1 1 1 2 2

and their function as a series of suffixes only:

1 2 34 35 45

omitting +. However 10, 11, 12, 13, 14 and 15 are expressed by K, S, N, J, F and L; respectively, in order to avoid confusion between a two digit number and two one digit numbers.

Returning to B1, the next partition of $V$ is generated and the above process is repeated. When all partitions of $V$ are exhausted, the control of the program is transferred to B7, increasing $T$ by 1 and returning to B1. If $T=V$, the computer stops at B8.

### (b) A Subroutine to Generate Partitions of a Number

A subroutine to generate partitions of a given number, and also their total sum; that is, a partition number, was made primarily for this purpose and incorporated into the library of the parametron computer MUSASINO-1, being entitled as $V\alpha_1$. The program with 50 words, is shown in Table 1.

**Table 1**

SUBROUTINE TO GENERATE PARTITIONS OF A NUMBER

For the instruction orders of the parametron computer MUSASINO-1, see "The High Speed Computation of $e$ by the MUSASINO-1" in Reports of ECL, Vol. 7, No. 6, pp. 192–198, June 1959.

| Address | Order | | Content |
|---|---|---|---|
| 0 | +5 ( )F<br>42 43L | | Link |
| 1 | 36 3L<br>L5 49L | — | Discrimate if J or 5 |
| 2 | 42 19L<br>46 42L | | |
| 3 | 00 7F<br>01 12F | ← | |
| 4 | 40 F<br>L0 1S3 | | Is it new $V$? |
| 5 | N6 20L<br>L5 20L | | |
| 6 | 46 12L<br>46 13L | | |

**Table 1**

| Address | Order | | Content |
|---|---|---|---|
| 7 | L5 F | | Set new $V$ |
| | 40 2S3 | | |
| 8 | 42 1S3 | | Set constants |
| | L4 7L | | |
| 9 | 42 48L | | |
| | 42 F | | |
| 10 | 00 20F | | |
| | 46 48L | | |
| 11 | L0 44L | | |
| | 46 L | | |
| 12 | L5 ( )F | ← | Erase |
| | N6 16L | — | |
| 13 | 41 ( )F | | |
| | L5 12L | | |
| 14 | L4 44L | | |
| | 46 12L | | |
| 15 | 46 13L | | |
| | 26 12L | — | |
| 16 | L5 5F | ← | Check if memory space for partitioned number is exhausted. |
| | L0 F | | |
| 17 | 36 18L | — | |
| | FF F | | |
| 18 | 41 S3 | ← | |
| | F5 S3 | ← | Count a turn number of partitions of $V$. |
| 19 | 40 S3 | | |
| | 26 43L | | |
| 20 | F5 3S3 | | Increase $a_2$ by one. |
| | 40 3S3 | | |
| 21 | L5 2S3 | | Subtract one from $a_2$. |
| | L0 41L | | |
| 22 | 42 2S3 | | Is $a_2 \leqq a_1$? |
| | L0 3S3 | | |
| 23 | 00 28F | | |
| | 32 18L | — | |
| 24 | L5 45L | | If $a_2 > a_1$, increase $a_i$ by one ($i \geqq 3$). |
| | 40 25L | | |
| 25 | F5 ( )F | | |
| | 40 ( )F | | |
| 26 | 40 F | | Set $a_{i-1}=a_{i-2}=\cdots\cdots=a_2=a_i$. |
| | L5 25L | | |
| 27 | L0 41L | | |
| | 42 28L | | |
| 28 | L5 F | | |
| | 40 ( )F | | |
| 29 | L5 28L | | |
| | L0 46L | | |
| 30 | N2 31L | — | |
| | L5 28L | | |
| 31 | 26 27L | | |
| | L5 L | ← | |
| 32 | 46 33L | | Calculate $V-(a_i+\cdots\cdots+a)$. |
| | L5 1S3 | | |
| 33 | L0 ( )F | ← | |
| | 40 F | | |
| 34 | L5 33L | | |
| | L0 44L | | |
| 35 | 46 33L | | |
| | L0 47L | | |
| 36 | N2 37L | — | |
| | L5 F | | |
| 37 | 26 33L | — | |
| | L5 F | ← | Replace $a_1$ by $V-(a_i+\cdots\cdots+a_2)$ and check if it is larger than $a_2$. |
| 38 | 40 2S3 | | |
| | L0 3S3 | | |
| 39 | 32 18L | | |
| | F5 25L | | If not, increase $i$ by one. |
| 40 | L4 44L | | |
| | 40 25L | | |
| 41 | L0 48L | | |
| | 10 1F | | A constant |
| 42 | 36 S4 | | When all partitions of $V$ are exhausted, return to $S^4$. |
| | 26 25L | | |
| 43 | L5 S3 | | |
| | 22 ( )F | | →Main program |
| 44 | 00 1F | | Constants |
| | 00 F | | |
| 45 | F5 4S3 | | |
| | 40 4S3 | | |
| 46 | L5 F | | |
| | 40 3S3 | | |
| 47 | L0 2S3 | | |
| | 40 F | | |
| 48 | F5 ( )F | | |
| | 40 ( )F | | |
| 49 | 00 43L | | |
| | 00 20L | | |

This subroutine can be used in two ways.

i) When all possible partitions of $V$ are to be generated successively, this subroutine is placed at address $q$ and entered from the main program with the following entry;

| Address | Order |
|---|---|
| | 50 $VF$ |
| $p$ | 50 $pF$ |
| $p+1$ | 26 $qF$ |

The integers according to a partition of $V$ are placed in a series of addresses specified by a present parameter, where $a_i$ is an integer placed in an address $i$ and the relation

$$a_1 \geqq a_2 \geqq a_3 \geqq \tag{5}$$

is maintained.

For each use of the subroutine, a new partition is obtained. For example, if $V$ is

4, the first calculation will give 4, the second 3 and 1; the third 2 and 2; the fourth 2, 1, and 1; the fifth 1, 1, 1, and 1.

ii) When only the number of different partitions of $V$ is required and individual partions are not required, the subroutine should be entered with the following entry:

| Address | Order |
|---|---|
| $p$ | 50 $VF$<br>50 $qF$ |
| $p+1$ | 26 $qF$ |

Then, the subroutine checks all possible partitions of $V$ and puts the sum in an accumulator. However, this case is not necessary for this paper.

A process to generate a partition in the case ($i$), is as follows:

i) Numbers in a series of addresses are set as follows:

$$a_1=V, \quad a_2=a_3=\cdots\cdots=0.$$

ii) Replace $a_2$ by $a_2+1$, $a_1$ by $a_1-1$ and check which of these new $a_1$ and $a_2$ is larger. If $a_1 \geqq a_2$, $a_1$, $a_2$, $a_3\cdots\cdots$given the required partition.

iii) If $a_1<a_2$, replace $a_i$ by $a_i+1$. ($i$ was set in the beginning but will be increased by ($V$)). Replace all of $a_2$, $a_3$,$\cdots\cdots$, $a_i-1$ by this new $a_1$ and calculate $V-(a_2+\cdots\cdots+a_i)$ for the next step.

iv) Replace $a_1$ by $V-(a_2+\cdots\cdots+a_i)$ and check whether this or $a_2$ is larger. If $V-(a_2+\cdots\cdots+a_i)\geqq a_2$, then $a_1$, $a_2$, $a_3$ are the required partitions.

v) If $V-(a_2+\cdots\cdots+a_i)<a_2$, replace $i$ by $i+1$ and return to iii). When a partition of $i=V$, that is, $a_1=a_2=\cdots\cdots=a_i=1$, is given generation ends.

### 4. Expressions of Functions Representable by a Single Element

By (2) and (3), the total coupling number K can be calculated from $V$ and $T$. For a constant input of zero,

$$K=2T-1 \tag{6}$$

and for a constant input of one,

$$K=2(V-T)+1. \tag{7}$$

The former is independent of $V$ and if $T$ is small, so is $K$. Therefore from the function expressions obtained by the program in the previous section, Table 2 was obtained. It lists function expressions which are not representable for smaller $T$ in a case where the constant input is zero. All $V$'s are traced increasingly. This implies that a function is not representable by a coupling number smaller $K$ than the listed value.

Functions which are representable with a constant input of one are dual to those with a constant input of zero. Therefore a function which is representable by a minimum coupling number in the latter case, is also a representable coupling number, even in the former case. This property was taken into account in making Table 2.

Table 2 shows a fairly complex situation. From this table we can see the minimum total coupling number required for realization of a function by a single element. For example, the function:

12+134+234+135+235+145+245 can be realized by a single element with $V+11$, $T=6$, $\omega_1=\omega_2=3$, $\omega_3=\omega_4=2$, $\omega_5=1$; that is, $K=11$ but from Table 2 we can see that this function can be realized with coupling number $K=7$, which is less than the previous case by four; that is, with $V+7$, $T=4$, $\omega_1=\omega_2=2$, $\omega_3=\omega_4$, $\omega_5=1$ and that this can not be realized with a lower coupling number. Fuctions of up to $V+12$ are listed in this table checked by the computer. For $n=2$, 3 and 4, all functions are exhausted in this table but for $n=5$, some functions are representable by values

**Table 2**

FUNCTIONS REPRESENTABLE BY SINGLE ELEMENTS

| Number of Variables | $V$ | $T$ | Coupling Numbers of Variables | $K$ | Function |
|---|---|---|---|---|---|
| 2 | 2 | 1 | 11 | 3 | 1+2 |
| 2 | 2 | 2 | 11 | 3 | 12 |
| 3 | 3 | 1 | 111 | 5 | 1+2+3 |
| 3 | 3 | 2 | 111 | 3 | 12+13+23 |
| 3 | 3 | 3 | 111 | 5 | 123 |
| 3 | 4 | 2 | 112 | 5 | 1+23 |
| 3 | 4 | 3 | 112 | 5 | 12+13 |
| 4 | 4 | 1 | 1111 | 7 | 1+2+3+4 |
| 4 | 4 | 2 | 1111 | 5 | 12+13+23+14+34+24 |
| 4 | 4 | 3 | 1111 | 5 | 123+124+134+234 |
| 4 | 4 | 4 | 1111 | 7 | 1234 |
| 4 | 5 | 2 | 1112 | 7 | 1+23+24+34 |
| 4 | 5 | 3 | 1112 | 5 | 12+13+14+234 |
| 4 | 5 | 4 | 1112 | 7 | 123+124+134 |
| 4 | 6 | 2 | 1122 | 9 | 1+2+34 |
| 4 | 6 | 3 | 1122 | 7 | 12+13+23+14+23 |
| 4 | 6 | 3 | 1113 | 7 | 1+234 |
| 4 | 6 | 4 | 1113 | 7 | 12+13+14 |
| 4 | 6 | 4 | 1122 | 7 | 12+134+234 |
| 4 | 6 | 5 | 1122 | 9 | 123+124 |
| 4 | 7 | 3 | 1123 | 9 | 1+23+24 |
| 4 | 7 | 5 | 1123 | 9 | 12+134 |
| 4 | 8 | 4 | 1223 | 9 | 12+13+23+14 |
| 4 | 8 | 5 | 1223 | 9 | 12+13+234 |
| 5* | 5 | 1 | 11111 | 9 | 1+2+3+4+5 |
| 5 | 5 | 2 | 11111 | 6 | 12+13+23+14+24+34+15+25+35+45 |
| 5 | 5 | 3 | 11111 | 5 | 123+124+134+234+125+135+235+145 +245+345 |
| 5 | 5 | 4 | 11111 | 6 | 1234+1235+1245+1345+2345 |
| 5 | 5 | 5 | 11111 | 9 | 12345 |
| 5 | 6 | 2 | 11112 | 9 | 1+23+24+34+25+35+45 |
| 5 | 6 | 3 | 11112 | 7 | 12+13+14+234+15+235+245+345 |

**Table 2**

| Number of Variables | $V$ | $T$ | Coupling Numbers of Variables | $K$ | Function |
|---|---|---|---|---|---|
| 5 | 6 | 4 | 11112 | 7 | 123+124+134+125+135+145+2345 |
| 5 | 6 | 5 | 11112 | 9 | 1234+1235+1245+1345 |
| 5 | 7 | 2 | 11122 | 11 | 1+2+34+35+45 |
| 5 | 7 | 3 | 11113 | 9 | 1+234+235+245+345 |
| 5 | 7 | 3 | 11122 | 9 | 12+13+23+14+24+15+25+345 |
| 5 | 7 | 4 | 11113 | 7 | 12+13+14+15+2345 |
| 5 | 7 | 4 | 11122 | 7 | 12+134+234+135+235+145+245 |
| 5 | 7 | 5 | 11113 | 9 | 123+124+134+125+135+145 |
| 5 | 7 | 5 | 11122 | 9 | 123+124+1251+345+2345 |
| 5 | 7 | 6 | 11122 | 11 | 1234+1235+1245 |
| 5 | 8 | 2 | 11222 | 13 | 1+2+3+45 |
| 5 | 8 | 3 | 11123 | 11 | 1+23+24+25+345 |
| 5 | 8 | 3 | 11222 | 11 | 12+13+23+14+24+34+15+25+36 |
| 5 | 8 | 4 | 11114 | 9 | 1+2345 |
| 5 | 8 | 4 | 11123 | 9 | 12+13+14+234+15+235+245 |
| 5 | 8 | 4 | 11222 | 9 | 12+13+23+145+245+345 |
| 5 | 8 | 5 | 11114 | 9 | 12+13+14+15 |
| 5 | 8 | 5 | 11123 | 9 | 12+134+135+145+2345 |
| 5 | 8 | 5 | 11222 | 9 | 123+124+134+234+125+135+235 |
| 5 | 8 | 6 | 11123 | 11 | 123+124+125+1345 |
| 5 | 8 | 6 | 11222 | 11 | 123+1245+1345+2345 |
| 5 | 8 | 7 | 11222 | 13 | 1234+1235 |
| 5 | 9 | 3 | 11133 | 13 | 1+2+345 |
| 5 | 9 | 3 | 11223 | 13 | 1+23+24+34+25+35 |
| 5 | 9 | 4 | 11124 | 11 | 1+234+235+245 |
| 5 | 9 | 4 | 11133 | 11 | 12+13+23+14+24+15+25 |
| 5 | 9 | 4 | 11223 | 11 | 12+13+23+14+15+245+345 |
| 5 | 9 | 5 | 11223 | 9 | 12+13+234+235+145 |
| 5 | 9 | 6 | 11124 | 11 | 12+134+135+145 |
| 5 | 9 | 6 | 11133 | 11 | 12+1345+2345 |
| 5 | 9 | 6 | 11223 | 11 | 123+124+134+125+135+2345 |
| 5 | 9 | 7 | 11133 | 13 | 123+124+125 |
| 5 | 9 | 7 | 11223 | 13 | 123+1245+1345 |
| 5 | 10 | 3 | 11233 | 15 | 1+2+34+35 |

Table 2

| Number of Variables | $V$ | $T$ | Coupling Numbers of Variables | $K$ | Function |
|---|---|---|---|---|---|
| 5 | 10 | 4 | 11134 | 13 | 1+23+24+25 |
| 5 | 10 | 4 | 11224 | 13 | 1+23+245+345 |
| 5 | 10 | 4 | 12223 | 13 | 12+13+23+14+24+34+15 |
| 5 | 10 | 5 | 11224 | 11 | 12+13+14+234+15+235 |
| 5 | 10 | 5 | 11233 | 11 | 12+13+23+145+245 |
| 5 | 10 | 5 | 12223 | 11 | 12+13+14+234+235+245+345 |
| 5 | 10 | 6 | 11224 | 11 | 12+13+145+2345 |
| 5 | 10 | 6 | 11233 | 11 | 12+134+234+135+235 |
| 5 | 10 | 6 | 12223 | 11 | 123+124+134+234+125+135+145 |
| 5 | 10 | 7 | 11134 | 13 | 12+1345 |
| 5 | 10 | 7 | 11224 | 13 | 123+124+134+125+135 |
| 5 | 10 | 7 | 12223 | 13 | 123+124+134+2345 |
| 5 | 10 | 8 | 11233 | 15 | 123+1245 |
| 5 | 11 | 4 | 12233 | 15 | 12+13+23+14+24+34+15+25 |
| 5 | 11 | 5 | 11225 | 13 | 1+234+235 |
| 5 | 11 | 5 | 11234 | 13 | 12+13+23+14+15+245 |
| 5 | 11 | 5 | 12233 | 13 | 12+13+23+14+24+345 |
| 5 | 11 | 7 | 11225 | 13 | 12+13+145 |
| 5 | 11 | 7 | 11234 | 13 | 12+134+135+2345 |
| 5 | 11 | 7 | 12233 | 13 | 123+124+134+234+125 |
| 5 | 11 | 8 | 12233 | 15 | 123+124+1345+2345 |
| 5 | 12 | 4 | 12234 | 17 | 1+23+24+34+25 |
| 5 | 12 | 5 | 11235 | 15 | 1+23+245 |
| 5 | 12 | 5 | 12234 | 15 | 12+13+23+14+24+15+345 |
| 5 | 12 | 6 | 11334 | 13 | 12+13+23+145 |
| 5 | 12 | 6 | 12225 | 13 | 12+13+14+234+15 |
| 5 | 12 | 6 | 12234 | 13 | 12+13+14+234+235+245 |
| 5 | 12 | 6 | 22233 | 13 | 12+134+234+135+235+145+245+345 |
| 5 | 12 | 7 | 11334 | 13 | 12+13+234+235 |
| 5 | 12 | 7 | 12225 | 13 | 12+13+14+2345 |
| 5 | 12 | 7 | 12234 | 13 | 12+134+234+135+145 |
| 5 | 12 | 7 | 22233 | 13 | 123+124+134+234+125+135+235+145 +245 |
| 5 | 12 | 8 | 11235 | 15 | 12+134+135 |
| 5 | 12 | 8 | 12234 | 15 | 123+124+134+135+2345 |

**Table 2**

| Number of Variables | $V$ | $T$ | Coupling Numbers of Variables | $K$ | Function |
|---|---|---|---|---|---|
| 5 | 12 | 9 | 12234 | 17 | 123+124+1345 |

* A case of $n=5$ includes the following sixteen functions besides the above.

| Number of Variables | Function |
|---|---|
| 5 | 123+134+125+134 |
| | 135+142+234+235+245+345 |
| | 125+134+135+145+234+235+245+345 |
| | 12+13+14+15+25 |
| | 13+23+24+34+35+45 |
| | 12+134+135+234 |
| | 12+135+245+234+235+245 |
| | 12+234+1345 |
| | 12+23+134+245 |
| | 12+23+134+135+145+245 |
| | 12+23+134+135+145+245+345 |
| | 12+13+14+234+235 |
| | 1+25+35+234 |
| | 13+15+25+14+234 |
| | 12+15+25+14+234+345 |
| | 12+15+2345 |

of $V$ geater than 13. These were not caught by this program. These were determined by a different method and are listened at the end of Table 2. The only value of $V$ greater than 13 is 16. Then numbers of functions of variables up to 5 which is representable by a single element are as follows:

| $n$ | Number of Functions of $n$ Variables |
|---|---|
| 2 | 2 |
| 3 | 5 |
| 4 | 17 |
| 5 | 92 |

Here each listed number of function does not include functions of variables less than $n$. These numbers were checked by another method which does not relay on a computer progam and will be described elsewhere.

The above program for $V$ up to 12 required about 30 hours on our parametron computer MUSASINO-1. However the computer has only a 256 word magnetic core memory at the present time and this limited capacity greatly restricted programming.

## Conclusions

More non-numerical problems like those in the present paper will be dealt with by computers in the future. However, as there is no standard technique as is in numerical analysis, programming techniques may greatly limit the effectiveness of computers. The author hopes that this paper clarifies certain aspects of a problem of a nature.

* * * *

621. 315. 592:548. 3]:536. 21. 083

# Measurement of Thermal Conductivity in Semiconductors*

***Riro NII***†

*Thermal conductivity of $Bi_2Te_3$, PbTe and InSb was determined by a modified Ångström method in the temperature range of 100°–600° K. A heat source whose temperature varied sinusoidally with time was used. Samples used were all single crystals, with their dimensions being $0.3 \times 0.3$ cm² in cross section and $0.2-0.8$ cm in length. They were soldered to the heat source. A sinusoidal temperature wave traveled through them and reflected at their ends. Two values of thermal conductivity were determined, one from the amplitude ratio and the other from the phase difference at both ends of the sample. These two values agreed very well. The results obtained by this method differed from those determined by Joffé and Devyatkova for PbTe.*

## Introduction

In general, thermal conductivity $K$ may be written as the sum of two components: $K_g$, the lattice thermal conductivity and $K_e$, the thermal conductivity of charge carriers. At sufficiently high temperatures $K_g$ decreases as $1/T$. $K_e$ is usually considered to follow the Wiedemann-Franz law and it forms only a small part of the total thermal conductivity $K$ in the case of semi-conductors. In 1954 Busch and Schneider(1) found an anomalous behavior in the thermal conductivity of InSb. It did not decrease as $1/T$. There was a minimum at about 400° K and this was considered to be due to an anomalously large contribution of charge carriers to the thermal conductivity. Price(2) assumed that the heat conduction was caused by the ambipolar diffusion of electrons and holes at higher temperatures. Although he obtained a larger contribution of charge carriers than that given by the Wiedomann-Franz law, the experimental values were too large to be explained by this assumption. Recently Stuckes(3) measured it by a comparison method. His results were quite different from those obtained by Busch Schneider. The absolute values were about a quarter those of Busch and Schneider, and there was no minimum in their temperature dependence. This shows that the measurement of thermal conductivity is very difficult because of the heat loss by radiation and conduction through lead wires. It is important to carry out experiments by various methods and compare the results with those obtained by many experimenters. $Bi_2Te_3$ is one of the typical semiconductors on which most careful experiments have been made,(4)(5) and the results thus obtained were in good quantitative agreement with the theory of Price. Therefore, $Bi_2Te_3$ was chosen as the test specimen for this research. In 1956 Joffé(6) published the thermal conductivity of PbTe and showed that the heat conduction due to excitons might form a considerable part of the thermal conductivity in the higher temperature range. It was considered worth while carrying out the measurement again in PbTe by a method quite different from that of Joffé.

## 1. Method of Measurement

In the Ångström method,(7) a semi-infinite thin rod is used, of which one end is in thermal contact with a heat source whose temperature varies sinusoidally with time. The fundamental equation for the temperature $\theta$ in the rod which, in addition to conducting heat, is radiating heat to its surroundings is

---

* Parts of this paper appeared in the *Jour. Phys. Soc. Japan*, Vol. 18, pp. 769–770, 1958.

† Semiconductors Research Section.

$$k\frac{\partial^2\theta}{\partial x^2}=\frac{\partial\theta}{\partial t}+\mu\theta \qquad (1)$$

where $x$ is the length measured along the rod, $t$ is time $\mu$ is the radiation constant, and $k$ is the thermal diffusivity; which is related to the thermal conductivity $K$ by the relation

$$K=kcd$$

where $c$ is the specific heat and $d$ is the density. The boundary condition is

$$\left.\begin{array}{ll}\theta(0,t)=A_0+A_1\cos\omega t & \text{at}\quad x=0\\ \theta=0 & \text{at}\quad x=\infty\end{array}\right\}. \qquad (2)$$

The general solution is

$$\theta(x,t)=A_0\exp(-\alpha_0 x)$$
$$+A_1\exp(-\alpha_1 x)\cos(\omega t-\beta_1 x), \qquad (3)$$

where

$$\alpha_0=\mu/k$$

$$\alpha_1=\{(1/2k)[(\mu^2+\omega^2)^{1/2}+\mu]\}^{1/2} \qquad (4)$$

$$\beta_1=\{(1/2k)[(\mu^2+\omega^2)^{1/2}-\mu]\}^{1/2}. \qquad (5)$$

Eliminating $\mu$ from Eqs. (4) and (5), we obtain:

$$\alpha_1\beta_1=\omega/2k. \qquad (6)$$

By measuring $\alpha_1$ and $\beta_1$ from the damping and phase change of the temperature wave at two points on the rod, $k$ may be determined from this formula. In this method, it is not necessary to measure heat powers generated at the source, but the specific heat of the sample must be known to calculate the thermal conductivity $K$ from the thermal diffusivity $k$.

Since the samples of semiconductors are of small dimensions, particularly when single crystals are used, the above method must be modified as follows. Now, the samples are used in the form of small cubes. They are in thermal contact with the heat source mentioned above. Then the temperature wave reflects at their ends. If heat loss is neglected, the boundary condition will be changed to:

$$\left.\begin{array}{ll}\theta(0,t))=A_0+A_1\cos\omega t & \text{at}\quad x=0\\ d\theta/dx=0 & \text{at}\quad x=l\end{array}\right\} \qquad (7)$$

where $l$ is the length of a side of the cube. The second term of Eq. (7) means that heat flow is perfectly stopped and there is no temperature gradient at the end.

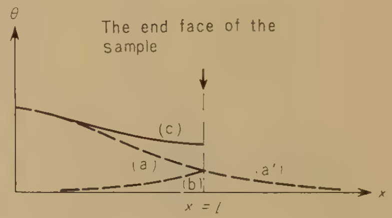


**Fig. 1**—(a)-(a′):The temperature distribution for a semi-infinite sample. (b): the mirror image of (a′). (c): the resultant temperature distribution.

Fig. 1 shows the temperature distribution as a function of $x$ at one instant of time. If (a) and (a′) are the temperature waves when the length of the samples is semi-infinite, the reflected wave (b), which is the image of (a′), will be the solution of Eq. (1). The resultant wave (c), which is the composite of (a) and (b), is also a solution of Eq. (1), and if $\omega$ and $l$ are chosen to have proper values, (b) will not reach to the heat source. Then the boundary condition of Eq, (7) will be fulfilled. The solution at $x=l$ is therefore,

$$\theta(l, t) = A_0 + 2A_1 \exp(-\alpha_1 l) \cos(\omega t - \beta_1 l) \quad (8)$$

$$\alpha_1 = \beta_1 = (\omega/2k)^{1/2}. \quad (9)$$

Here the radiation constant $\mu$ is set equal to zero in the previous equations. If $\alpha_1$ and $\beta_1$ are determined from the amplitude ratio and phase difference of the temperature wave at $x=0$ and $x=l$, $k$ may be calculated in two ways; either from $\alpha_1$ or $\beta_1$. These two solutions of $k$ from Eq. (9) must be the same, or there is some heat loss and the assumption that $\mu=0$ is not fulfilled.

### 2. Apparatus

The apparatus used for our measurements is shown schematically in Fig. 2. The measurements were made in a cylindrical copper can whose dimensions were 4 cm in diameter 10 cm in depth and 0.1 cm in thickness. It was used as a radiation shield. It carried heater $I_2$, which was made of nichrome wire, through which the temperatures of measurement were controlled. Th sample was soldered on the copper disk Thermocouples $T_1$ and $T_2$, which were mad of Copper-constantan, 0.01 cm in diameter were soldered to both ends of the sample Heater $I_1$ which was made of constantan 0.01 cm in diameter, was wound on a copper bar whose diameter was 0.1 cm, and an on off current power of 0.5 watts was passed through it. The period of the current was about 4 seconds. The thermal emfs. of $T$ and $T_2$ varied sinusoidally with time. A spring of constantan, 0.01 cm in diameter, was used for supporting the sample when the solder was melted at higher temperatures. The whole assembly was inserted in a glass tube and evacuated to about $10^{-3}$ mmHg. In a vacuum of $10^{-5}$ mmHg, no remarkable change could be seen in the results. In making low temperature measurements, the glass tube was immersed in liquid nitrogen. In the temperature range of 100–700° K the temperature differences of various parts of the apparatus were

$$T_{1\,\text{mean}} - T_{2\,\text{mean}} < 1^\circ\,\text{C}$$

$$T_3 - T_{2\,\text{mean}} < 5^\circ\,\text{C}.$$

The amplitude of the temperature wave at $T_1$ was about 1° C.

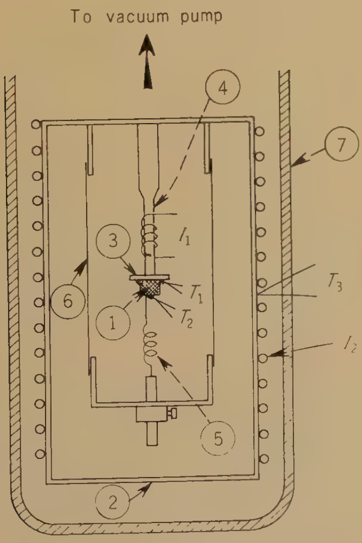


**Fig. 2**—Apparatus used for the measurement of Thermal Conductivity. ①: sample ②: copper can ③: copper disk ④: copper bar ⑤: constantan spring ⑥: mica support ⑦: glass tube.

### 3. Method of Measurement

The thermocouples $T_1$ and $T_2$ were connected to the circuit as shown in Fig. 3. The mean emfs. of the thermocouple pair were balanced by a potentiometer, which is seen on the right side of the figure. The sinusoidal component was detected by the periodic deflection of the Galvanometer. On the left side of the figure is a mechanical very-low-frequency oscillator which generated an accurate sinusoidal voltage in series with the thermocouple. The motor of this mechanical oscillator drove at the same time the on-off switch of heater $I_1$, which generated the temperature wave. The phase relation between the two could be changed by a mechanical phase shifter. When the amplitude and phase of the oscillator were suitablly chosen; the deflection of the galvanometer diminished to zero amplitude. The amplitude and phase of the thermal emfs. of thermocouples $T_1$ and $T_2$ were determined by this procedure.

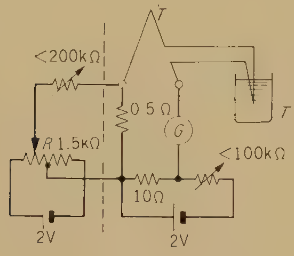


**Fig. 3**—Circuit used for the measurement of Thermal Conductivity $T$: thermocouple $T_s$: melting ice bath for reference junction $R_s$: this sliding contact moved to and fro by means of a cam driven by a motor.

### Conclusion

A typical example of the temperature dependence of $1/k$ of a $Bi_2Te_3$ single crystal is shown in Fig. 4. The dimensions of the sample were $0.35 \times 0.25$ cm$^2$ in cross section and 0.218 cm in length. The direction of the heat flow is parallel to the cleavage plane of the crystal. Symbol · shows the values calculated from the amplitude ratio and symbol × those calculated from the phase difference. It may be seen that these two values agree well with each other. The temperature dependence of its Hall coefficient $R$ and its resistivity $\rho$ is also shown in the figure. Since the specific heat of $Bi_2Te_3$ is not known, the thermal conductivity $K$ was not calculated. Therefore the absolute values cannot be compared with those of other authors'. But the temperature dependence is the same as that given by Goldsmid⁽⁴⁾ and by Satterthwaite and Ure.⁽⁵⁾

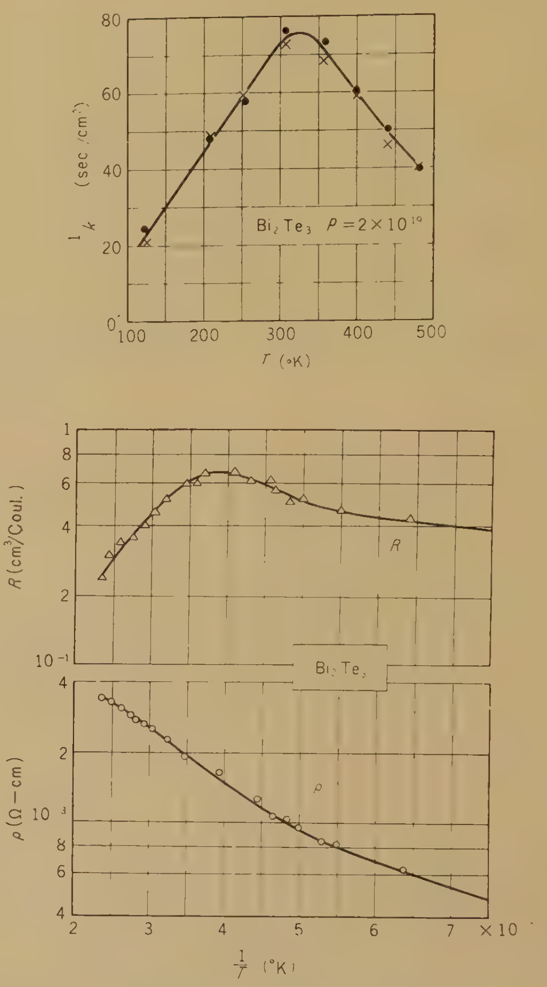


**Fig. 4**—The thermal and electrical properties of $Bi_2Te_3$. Symbol ● represents the value calculated from the amplitude ratio and × that from the phase difference.

The temperature dependence of $1/K$ of a PbTe single crystal, together with its electrical properties, is shown in Fig. 5. The sample was annealed for 62.5 hours in an evacuated and sealed glass tube at 800° K. Its dimensions were $0.28 \times 0.4$ cm$^2$ in cross section and 0.215 cm in length. The thermal conductivity was calculated from the values of $c$, which were given by Parkinson and Quarrington⁽⁸⁾ for temperatures lower than room temperature. The value of 12 cal/mol was obtained for temperatures above room temperature by extrapolation. The value of 8.15 g/cm$^3$ was selected for density $d$. The

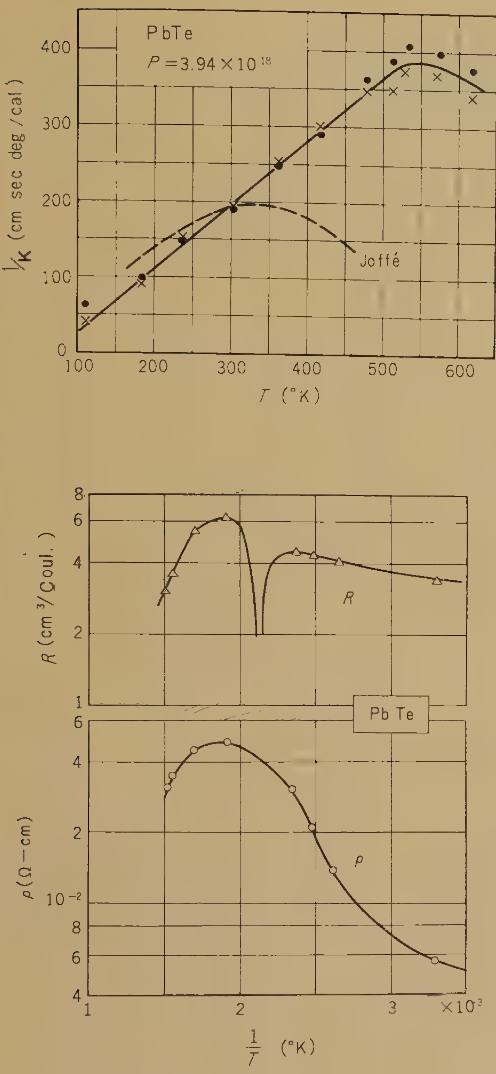


**Fig. 5**—The thermal and electrical properties of PbTe.

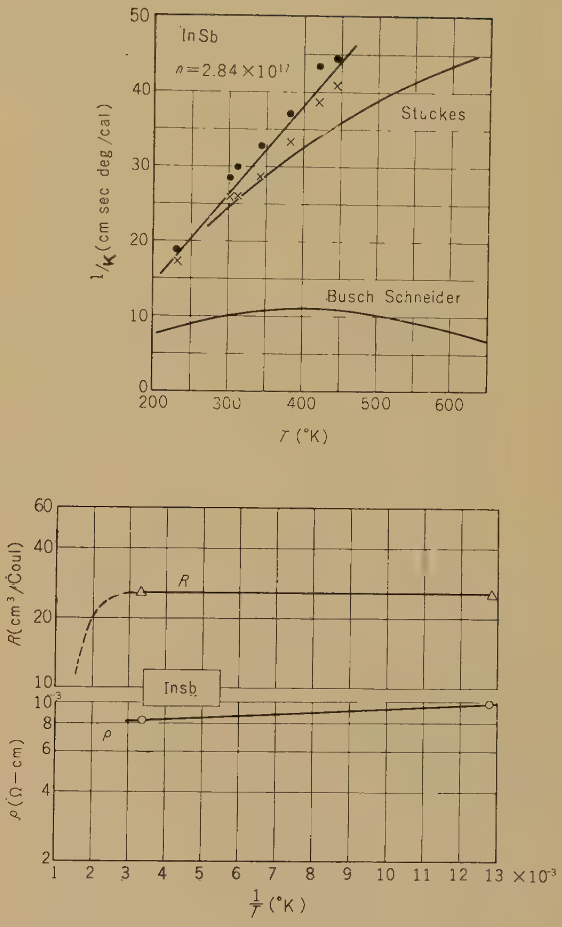


**Fig. 6**—The thermal and electrical properties of InSb.

dotted curve in Fig. 5 represents the results given by Joffé. In spite of the similarity of the electrical properties of Joffé's sample and ours, there is a rather large difference in behavior of the thermal conductivity at higher temperatures. The $1/K$ curve of our sample deviates from a straight line at higher temperatures, where the sample becomes intrinsic, and does not show any abnormal bend of thermal conductivity due to excitons. In this case, the reciprocals of thermal diffusivity $1/k$ are within the range of 15–120 sec/cm$^2$. These reciprocals have approximately the same range as those of $Bi_2Te_3$. The dimensions of both samples are also nearly equal, so that the experimental conditions for $Bi_2Te_3$ and PbTe may be considered almost identical except for the possible difference in radiation constant $\mu$. If the curve for PbTe really bends over near room temperature, it is difficult to understand why our experimental curve bends over for

$Bi_2Te_3$ but not for PbTe. Finally, a typical example of temperature dependence of $1/K$ of InSb single crystal and its electrical properties are shown in Fig. 6. In determining $K$, 12 cal/mol was assumed for the value of the specific heat and 5.777 g/cm$^3$ for the value of $d$. Measurement were made for two samples with different dimensions, one $0.25 \times 0.38$ cm$^2$ in cross section and 0.44 cm in length, and the other $0.27 \times 0.24$ cm$^2$ in cross section and 0.848 cm in length. The results were almost the same. For comparison, the results of Busch and Schneider,⁽¹⁾ and Stuckes⁽³⁾ are also shown here. It may be seen that our results are in good agreement with Stuckes' data.

**Acknowledgment**

The author wishes to express his sincere thanks to Mr. Y. Kanai for his suggestion of this problem and many valuable discussions. The author is also indebted to Mr. K. Mizuma for the samples of $Bi_2Te_3$. He would like to express his thanks to Dr. T. Niimi, the chief of the semiconductor research section, for the encouragement he has given to the author during the course of this work.

**References**

(1) Busch and Schneider, "Heat conduction in Semiconductors." *Physica*, 20, 11, p. 1084, 1954.

(2) P. J. Price, "Ambipolar thermodiffusion of electrons and holes in semiconductors." *Phil. Mag*, 46, 382, p. 1252, 1955.

(3) A. D. Stuckes, "Thermal conductivity of Indium Antimonide." *Phys. Rev.*, 107, 2, p. 427. 1957.

(4) H. J. Goldsmid, "The thermal conductivity of Bismuth Telluride." *Proc. Phys. Soc.*, B69, 2, p. 203, 1956.

(5) C. B. Satterthwaite and R. W. Ure, Jr. "The electrical and thermal properties of $Bi_2Te_3$." *Phys. Rev.*, 108, 5, p. 1164, 1957.

(6) A. F. Joffé, "Heat transfer in semiconductors." *Canadian Journal of Physics*, 34, 12, p. 1342, 1956.

(7) P. H. Sidles and G. C. Danielson, "Therma diffusivity of metals at high temperatures.' *J. A. Phys.*, 25, 1, p. 58, 1954.

(8) D. H. Parkinson and J. E. Quarrington, "The molar heats of Lead Sulfide, Selenide and Telluride in the temperature range 20° K to 260° K." *Proc. Phys. Soc.* A67, 7, p. 569, 1954.

(9) R. Nii, "Measurement of the thermal conductivity in semiconductors." *J. Phys. Soc. Japan*, 13, 7, p. 769–770, 1958.

(10) Y. Kanai and R. Nii, "Experimental studies on the thermal conductivity in semiconductors." *J. Phys. Chem. Solids*, 8, p. 338, 1959.

* * * *

621. 318. 57:621. 314. 7
621. 395. 345

# Semiconductor Speech-Path Switches Suitable for Direct-Coupled Connection*

*Ichiro ENDO*† and *Shoji YOSHIDA*†

*This paper describes three types of bilateral speech-path switches for all-electronic telephone exchange systems. The main object of this research was to obtain elementary semiconductor speech-path circuits which can be connected with each other directly, without using coupling circuits such as transformers or capacitors between stages. This feature is desirable for multistage connection in a large scale exchange system.*

*The first circuit uses a diode bridge, the second circuit uses grounded base p-n-p and n-p-n transistors connected alternately, and the third circuit uses a compound p-n-p-n transistor made up of one n-p-n transistor and one p-n-p transistor. For practical use, the last circuit seems to be the most promising.*

## Introduction

One of the most important problems in the realization of all-electronic telephone exchange systems is the selection of speech-path switches both technically and economically suitable for the system.

Various papers about electronic switches for speech-path circuits have been published at home and abroad, and the devices used in these switches have been vacuum tubes, semiconductor diodes, transistors, etc.

Speech-path switches, according to their construction, are generally classified into three types:

(a) Space-division switches,
(b) Time-division switches,
(c) Frequency-division switches.

Semiconductor switches considered in this paper belong to type (a). The main requirements for a switch of the space division type are ;

(1) It must have a high switching speed.
(2) It must have bilateral transmission characteristics. Accordingly, in the "on" state, its insertion loss in the voice frequency band must be sufficiently low, and it must be capable of transmitting a voice signal of several mW with no distortion.
(3) In the "off" state, its insertion loss in the voice frequency band must be extremely high.
(4) It must not generate any undesirable electronic noise.
(5) A self-holding switch is preferable, because a switch having this function can hold the "on" state without the aid of control signals while a conversation is continued.
(6) High stability must be maintained for a long period. Moreover, small size and high uniformity are desirable.
(7) Power dissipation must be small.

Generally speaking, in electronic switches, control and voice currents pass through a common path. In this respect electronic switches differ from electromechanical switches, in which the control and voice current paths are completely independent. To separate these two kinds of currents in

---

* MS (in Japanese) was received by the Electrical Communication Laboratory, Feb. 13, 1959 and published in the Kenkyu Zituyôka Hôkoku (*Electrical Communication Laboratory Technical Journal*), Vol. 8, No. 4, pp. 333–354, 1959.

† Switching Research Section.

circuits of electronic switches connected in series, coupling elements such as transformers, capacitors, and inductors are generally employed between switches. The use of such coupling elements necessarily results in increased insertion loss in the "on" state, in increased cost, and in increased space consumption. Accordingly, it is desirable that the switches be connected directly without using coupling elements. From this point of view, we chose three kinds of speech-path switches and conducted experiments on them. As a result it became known that they have satisfactory switching ratio, insertion loss and transmission level characteristics. One of the three switches possesses the self-holding function. The following sections treat mainly the transmission characteristics of these switches.

### 1. Methods of Coupling Speech-Path Switches Directly

To establish a cascade connection without using coupling elements, there are three methods as follows:

(a) By passing the control current through a route independent of the speech-path.
(b) By passing the control current through two adjacent switches.
(c) By passing the control current through cascaded switches regarded as a common control current path.

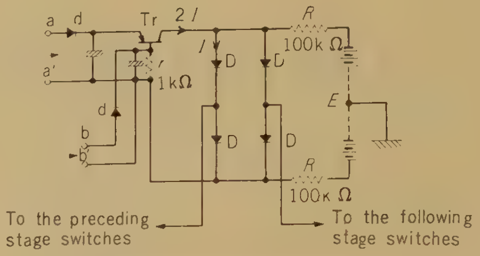
We utilized the following types of switches corresponding to the above methods.

(a) Diode-bridge switches.
(b) Base-controlled transistor switch chains where p-n-p and n-p-n transistors are arranged alternately.
(c) Compound p-n-p-n transistor switches employing one p-n-p transistor and one n-p-n transistor.

The networks and characteristics of these switches one illustrated in the following sections.

### 2. Diode-Bridge Switch

As shown in Fig. 1, a diode-bridge switch is constructed with four diodes of the same characteristics. If one of the two pairs of terminals of the diode-bridge is connected to the speech-path and the other pair of terminals to the control circuit, the speech-path is independent of the control-path. Therefore, such diode-bridges can be connected in cascade without coupling elements, and the control signal of a switch cannot flow into adjacent switches.


a
d
Tr
2 I
a'
I
D
D
R
100k Ω
1 kΩ
d
b
b'
D
D
E
R
100κ Ω
To the preceding stage switches
To the following stage switches

d: SD-16 gold bonded diode
D: ECL-1200 germanium junction diode
*E*: Reverse bias source

**Fig. 1**—Construction of the diode-bridge speech-path switch.

Also shown in Fig. 1 is a transistor circuit for controlling the switch. When a high frequency control signal appears across terminals *b* and *b′*, but not across terminals *a* and *a′*, then the transistor is in the cut-off region and the diode-bridge switch is in the "off" state. When the high frequency control signal on terminals *b* and *b′* disappears, and at the same time a signal appears across terminals *a* and *a′*, the switch enters the "on" state. A parametron flip-flop circuit is used for supplying this high frequency control signal.

The diodes employed in this switch were specifically designed and developed in our laboratory for this switch. They are germanium junction type diodes. Their reverse resistances are about 10 megohms at −10 volts and their forward resistances are low enough in the audio-frequency band (about 2 ohms at 20 milliamperes). Typical characteristics are shown in Fig. 2.

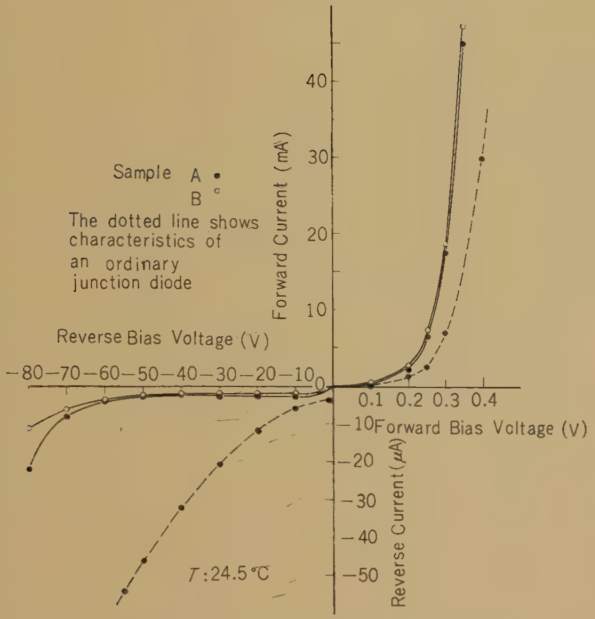


**Fig. 2**—Static-characteristics of ECL-1200 germanium junction diodes (two samples).

Fig. 3 illustrates their transmission characteristics. Voice signals up to a few milliwatts can be transmitted through the switches without appreciable distortion.

The advantages of this switch is the simplicity of speech-path circuit and the high switching ratio, though the control circuit of the switch is rather complicated.

### 3. Base-Controlled Transistor Switch

It is known that a symmetrical transistor switch(1) controlled by a polarity of the base potential, as shown in Fig. 4, has bilateral characteristics and a very high switching ratio. It therefore may be used as a speech-path switch. We have found a method of connecting such switches directly. As shown in Fig. 5, if transistor switches of p-n-p and n-p-n types are arranged alternately in adjacent stages, the control current of each switch establishes closed loop circuits with adjacent switches. Thus, such transistor switches can be connected without using coupling

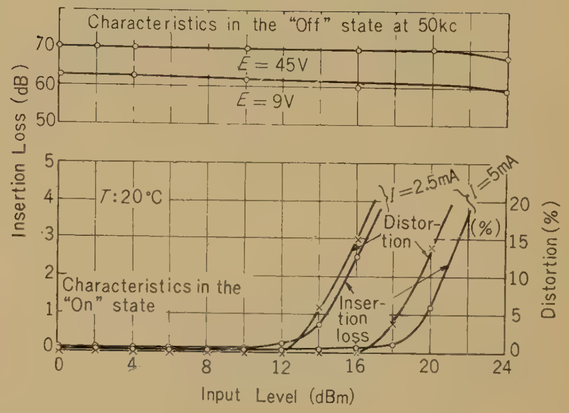


**Fig. 3 (a)**—Transmission characteristics of the diode-bridge switch.

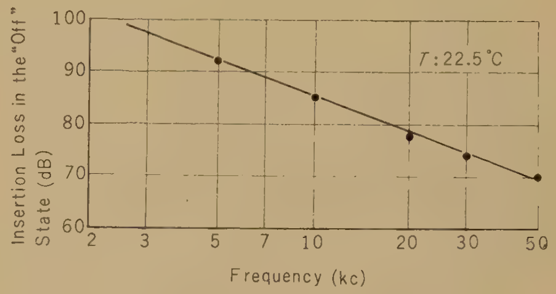


**Fig. 3 (b)**—Frequency characteristics of the insertion loss of the "off" diode-bridge switch (E=45 V).

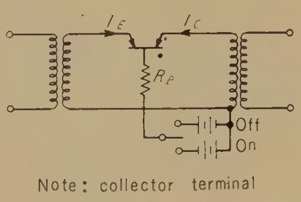


**Fig. 4**—P-n-p type symmetrical transistor switch.

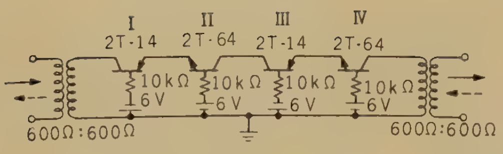


**Fig. 5**—Four-stage cascade connection of transistor switches.

elements.

By reversing the d-c voltage applied to the base of any switch shown in Fig. 5, the corresponding switch is turned off.

Transistors for switches of this type must have a bilateral current amplication factor sufficiently large to handle, with a small controlling power, large voice signals without introducing distortion or attenuation. In addition, a high bilateral current amplification factor is necessary for effective separation of the control circuit from the speech-path circuit. In our experiments, both symmetrical and nonsymmetrical (or general-purpose) transistors were used. However, nonsymmetrical transistors with approximately symmetrical properties were selected from among general-purpose transistors on the market.

Fig. 6 shows the characteristics in the case of four stage speech-path switches made of nonsymmetrical transistors. The insertion loss of the switch is about 0.25 decibels per stage.

## 4. Compound Transistor Switch

The circuit shown in Fig. 7 will be called a "compound transistor." It is constructed with complementary pairs of transistors (i.e. p-n-p and n-p-n), with the bases and the collectors of the pair interconnected.

It is noteworthy that this circuit has negative resistance characteristics like those of gas discharge diodes. This switch, therefore, has a self-holding function. The static characteristics of fundamental circuits and of cascaded circuits of compound transistors are illustrated in Fig. 8.

From the same figure, the following important facts can be ascertained.

Switches of this type can be connected in

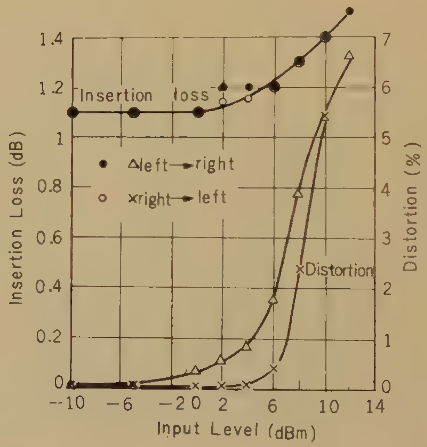
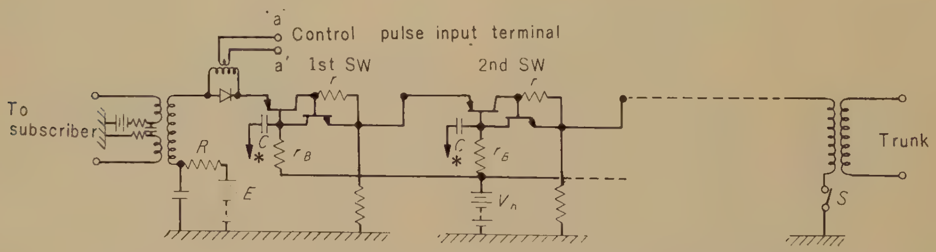


**Fig. 6**—Transmission characteristics of the circuit shown in Fig. 5 (*f*: 1 kc, *T*=28.5° C).



*To the rectangular wave source for lockout

**Fig. 7**—Cascade connection of compound transistor switches.

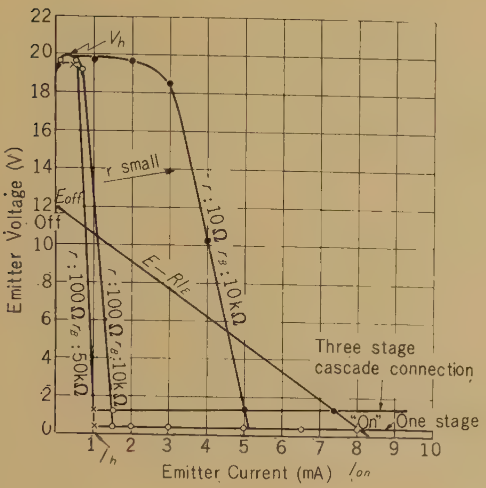
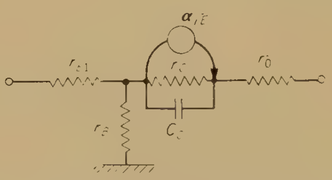


**Fig. 8**—$V-I$ characteristics of the compound transistor switch ($T_1$: $2T-14$, $T_2$: $2T-64$),

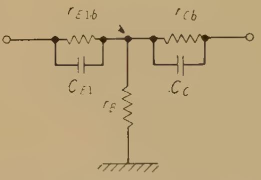
cascade without coupling elements between stages, and the breakdown voltage does not increase with the number of stages connected in cascade. This feature is different from those of gas discharge tubes and of p-n-p-n avalanche diodes.

In switches of this type using junction transistors for low frequency use, the "off" and the "on" impedances are above ten magohms and within several ohms respectively in the audio frequency range. Transmission characteristics and an equivalent circuit[(2)] of the compound transistor are shown in Fig. 9. With the application of a voltage pulse, by which the emitter potential of the first switch can exceed its base voltage, all switches connected in series conduct successfully like a lot of falling ninepins. On the other hand when they must be reset, they are all turned off at once by cutting off the conduction current at an arbitrary point in the speech-path switch series. Like gas discharge tubes, this switch series can be used with the so-called "end-marking" system in speech-path switch networks. That is, by the application of marking signals to both ends of a switch series, the route selection and the connection of a speech-path can be done automatically. Fig. 10 illustrates an example of a lockout method required for such an "end-marking" system. The occurrence of multiroutes can be suppressed by the resistance $R$ shown in Fig. 7.

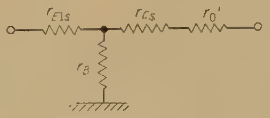
The lockout mechanism is as follows. As shown in Fig. 10, a rectangular wave of amplitude $\Delta V$ is applied continuously to the base of each switch through a common high value resistor $R_L$ in each column of



(a) Equivalent Circuit in the Active Region



(b) Equivalent Circuit in the Cutoff Region



(C) Equivalent Circuit in the Saturation Region

$C_{E1}$: EmitterCapacity of $T_1$, $r_{E1}, r_{E2}$: Emitter Resistances of $T_1$ and $T_2$, $r_{B1}, r_{B2}$: Base Resistances of $T_1$ and $T_2$, $r_{C1}, r_{C2}$: Collector Resistances of $T_1$ and $T_2$, $C_{C1}, C_{C2}$: Collector Capacities of $T_1$ and $T_2$, $r_{E1b}$: Emitter Resistance of $T_1$ in the "off" Region, $r_{E1s}, r_{E2s}$: Emitter Resistances of $T_1$ and $T_2$ in Saturation Region, $r_{C1s}, r_{C2s}$: Collector Resistances of $T_1$ and $T_2$ in Saturation Region, $\alpha_1, \alpha_2$: Current Amplification Factors of $T_1$ and $T_2$,

$\alpha=\alpha_1/(1-\sigma\alpha_2)$, $r_E=r_{E1}+(1-\alpha_1)r_{B1}$, $C_C'=C_{C1}+C_{C2}$, $C_C=C_C'/(1-\sigma\alpha_2)$, $r_C'=r_{C1}r_{C2}/(r_{C1}+r_{C2})$, $r_C=(1-\sigma\alpha_2)r_C'$, $r_0=\{r_{E2}+(1-\alpha_2)r_{B2}\}\sigma$, $\sigma=r/\{r_{E2}+(1-\alpha_2)r_{B2}+r\}$.

**Fig. 9 (a)**—Equivalent circuit for the compound transistor switch.

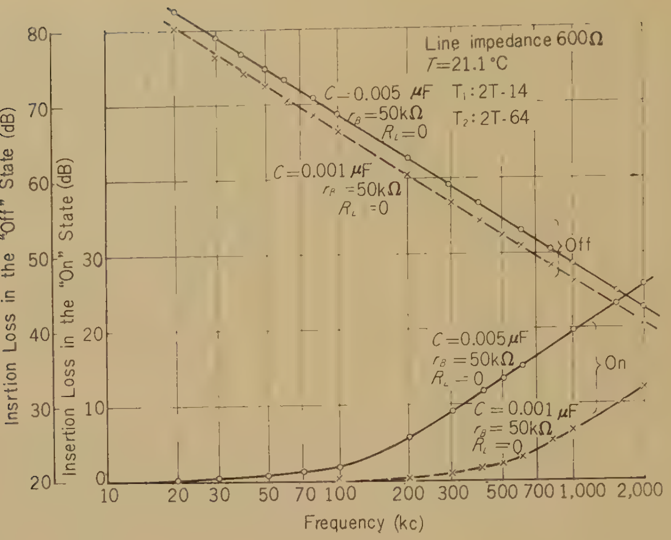


**Fig. 9 (b)**—Frequency characteristics of the compound transistor switch.

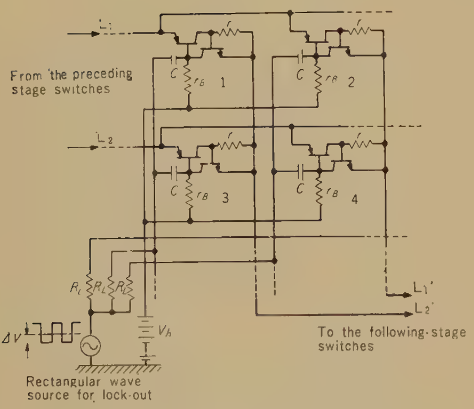

L₁
L₂
From the preceding stage switches
C
$r_B$
1
2
3
4
$R_L$
ΔV
$V_h$
L₁'
L₂'
To the following-stage switches
Rectangular wave source for lock-out

**Fig. 10 (a)**—Switch matrix.

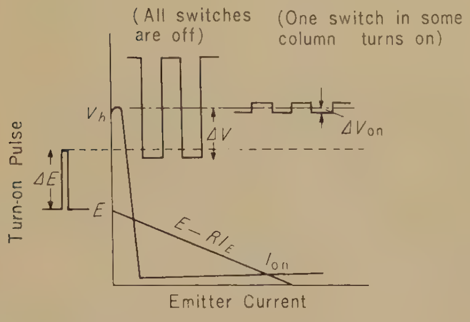


**Fig. 10 (b)**—Relation between the turn-on pulse and the rectangular wave signal for lockout.

the switch matrix. That is to say, when all switches are in the "off" state, the base potential changes with $\Delta V$. But when any one of the parallel switches connected to the common link ($L_1'$ or $L_2'$) is turned on, the base potentials of the others change with $\Delta V_{\mathrm{on}}$ because of voltage-drop through the common registor $R_L$. Furthermore, if the following relation exists:

$$V_h > V_h - \Delta V_{\mathrm{on}} > E + \Delta E > V_h - \Delta V > E,$$

where $V_h$ is the breakdown voltage of the switch, $E$ is the common d–c supply voltage of a switch series and $\Delta E$ is the amplitude of the trigger pulse applied, then a trigger pulse applied to the link $L_1$ turns on switch 1, and the base potential of switch 3 becomes $V_h \pm \Delta V_{\mathrm{on}}$, but the base potentials of switches 2 and 4 remain $V_h \pm \Delta V$. Therefore, if $-\Delta V$ is added to each base, and a trigger pulse is applied to $L_2$, then the base potential of switch 3, $V_h - \Delta V_{\mathrm{on}}$, becomes larger than $E + \Delta E$, and switch 3 cannot be turned on, though switch 4 can be turned on. Thus the undesirable cross connection of two or more speech-paths may be effectively avoided.

The time lengths required for the switch to be turned on or off are about 5 microseconds and 10 microseconds respectively, when transistors with an alpha cutoff frequency of 0.8 megacycles are used. When we conducted experiments on speech-path connections between a trunk and a subscriber through five stages of simplified networks with "end-marking" controls, the probability of occurrence of multiroutes for each connecting action was very small.

Thus, switches of this type were shown to have a self-holding function, and may be applied in "end-marking" switching networks. We may expect that using the system described, a considerable economy of both speech-path components and control components of electronic telephone exchange systems will be achieved.

## Conclusion

As described above, experiments were made on three kinds of multistage cascade connection circuits for speech-path switches using semiconductor devices. These circuits are desirable for construction of a system of speech-path switches on a large scale. These switches have the following characteristics.

Power consumption (in the "on" state): about 10 mW
Speech attenuation: below 0.3 dB
Maximum level of speech signals to be transmitted: about 10 dBm
Insertion loss (in the "off" state): over 90 dB

## References

(1) R. B. Trausdale, "The Symmetrical Transistor as a Bilateral Switching Element," *Communication and Electronics*, No. 26, p. 400. (1956-09).
(2) J. J. Ebers, "Four-Terminal P-N-P-N Transistors," *Proc. I.R.E.*, **40**, 11, p. 1361. (1952-11).

* * * *

621. 382. 2:261. 3. 011. 4

# The Nonlinear Barrier Capacitance of Silver Bonded Diodes*

**Shoichi KITA**† and **Koichi SUGIYAMA**†

*Recently the parametric amplifier has attracted attention because of its low noise characteristics. One of the authors has designed a new diode suitable for parametric amplifiers. This diode is a silver bonded diode which is composed of a silver-gallium whisker and an n-type germanium wafer. After the whisker makes contact with the germanium wafer, electrical forming is applied to make a silver bonded contact.*

*We measured the impedance variation of the diode as a function of bias voltage at 6 kMc by use of a coaxial standing wave meter. Barrier capacitance was calculated from this variation and this capacitance agreed with the theoretical values for reverse biases, but for forward biases the capacitance was larger than the theoretical value. The cut-off frequency of the diode was more than 400 kMc. The barrier capacitance variation factor,* $C_1/C_0$, *was four times larger than that of other point contact silicon and germanium diodes. It was discovered that electrical forming was the most important factor in determining the characteristics of the diode.*

*A 6 kMc parametric amplifier using a silver bonded diode was constructed. The bandwidth was 40 Mc at 20 dB gain and the noise figure was about 5 dB.*

## Introduction

Earlier, one of the authors discovered that welded contact germanium diodes showed negative resistance in the microwave region, and that they could be used for oscillation and amplification at 4 kMc.⁽¹⁾ Later it was proved that the amplification was due to a parametric excitation of the nonlinear barrier capacitance of the semiconductor diode.

The said author discovered in his experiments on a harmonic generator that a gold bonded germanium diode had a large nonlinear barrier capacitance in the negative bias region.⁽²⁾ And we succeeded in getting the microwave parametric amplification using gold bonded diodes. Recently, it was found that a silver bonded diode which had been designed by Kita and Nakayama was superior to the gold bonded diode for parametric amplification. We measured the barrier capacitance of the diode at 6 kMc. As the result, it was found that a barrier capacitance variation of the silver bonded diode was much larger than that of point contact diodes, such as 1N23B, and that the cut-off frequency of the diode was larger than 250 kMc. Electrical forming has been used in the process of manufacturing silver bonded diodes. This forming is necessary to obtain diodes with good characteristics.

We made a 6 kMc parametric amplifier using the silver bonded diode. The band width of the amplifier was 40 Mc at 20 dB gain and the noise figure was about 5 dB.

## 1. Diode used in experiments

The silver bonded diodes used in our experiments were made by the following process; after a silver whisker containing a small amount of gallium was brought into point contact with an $n$-type germanium wafer, an electrical forming current was applied to it by discharging current from a capacitor.

---

* This report was presented at the 1959 Electron Devices Meeting, Oct. 1959, and published in the *Journal of the Inst. Electr. Comm. Eng. Japan*, **42**, No. 12, pp. 1186–1192, Dec. 1959.

† Radio Section.

In general, during electrical forming a large current is passed through the diode one time; but we used a new method, in which the electrical forming was performed several times instead of once, the capacitor voltage was increased step by step. By this method diodes having a uniform characteristic could be easily obtained by observing the static characteristic with a cathod-ray oscilloscope. We measured the characteristics of the diodes which were constructed in a 1N23 type holder. We also used the 1N23B and point contact germanium diodes in our experiments.

## 2. Condition for the Parametric Oscillation of Semiconductor Diodes

In this section we will discuss the conditions for the parametric oscillation of semiconductor diodes. The equivalent circuit of the semiconductor diode is shown in Fig. 1, where $R_s$ is the spreading resistance, $R_B$ is the barrier resistance and $C_B$ is the barrier capacitance. When a reverse bias voltage is applied, $R_B$ becomes very high and the equivalent circuit includes only $R_s$ and $C_B$. The equivalent circuit of the diode whose breakdown voltage $V_B$ is low like that of a microwave diode is shown in Fig. 2, where $C_{\min}$ is a minimum capacitance at the breakdown voltage and $C$ a variable capacitance,

$$C_B = C + C_{\min}. \tag{1}$$

Let $\phi$ denote a contact potential difference at a contact point, and $V$ denote the applied voltage at the barrier. It has been found empirically that $C$ can be represented in the form of Eq. (2) (refer to Fig. 10):

$$C = \frac{C_c}{(\phi - V)^n}, \tag{2}$$

where $C_c$ and $n$ are constants.

Next, let

$$V = V_0 + V_1 \cos 2\omega t \tag{3}$$

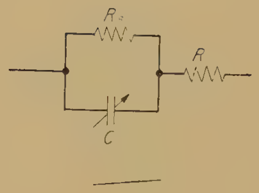


**Fig. 1**—Equivalent circuit of a diode.

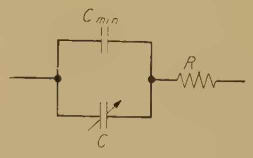


**Fig. 2**—Equivalent circuit of a diode with reverse bias voltage.

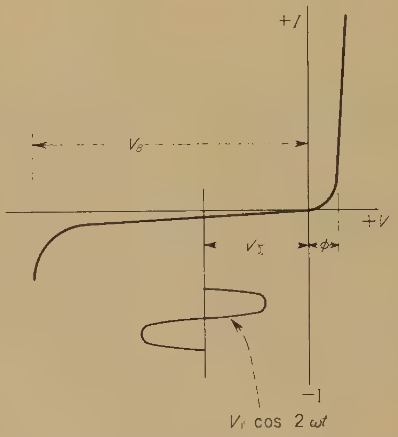


**Fig. 3**—The voltage which is applied to the barrier.

as shown in Fig. 3, where $V_0$ is the d.c. negative bias voltage, $V_1$ the maximum amplitude of the pump voltage and $\omega$ the angular frequency of the amplified signal. And if we assume

$$|V_1| < |V_0| \tag{4}$$

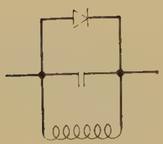


**Fig. 4**—Tuned circuit including a diode.

from Eqs. (1), (2), and (3), $C_B$ can be expanded into a Fourier series, and if the third and the subsequent terms are neglected:

$$C_B \doteqdot C_0 + 2C_1 \cos 2\omega t. \tag{5}$$

Inserting Eq. (3) into Eq. (2), and expanding Eq. (1) into a fourier series, we can find $C_0$ and $C_1$.

Ratio $C_1/C_0$ is

$$C_1/C_0 = \frac{nV_1}{2\{(\phi - V_0) + (C_{\min}/C_c)(\phi - V_0)^{n+1}\}}. \tag{6}$$

This ratio $C_1/C_0$ is an important factor for the properties of microwave paramntric amplifiers; the gain band product of the amplifiers is proportional to $C_1/C_0$.

Next, we consider conditions of oscillation when the diode is inserted in a turned circuit as shown in Fig. 4. If we neglect the resistive component of the circuit except that of the diode the $Q$ of the circuit is determined by the $Q$ of the diode, which is given by the following formula

$$Q = \frac{1}{\omega C_B R_s}. \tag{7}$$

The value of $C_B$ decreases as the negative bias voltage becomes larger and this value becomes $C_{\min}$ at the bias voltage $V_B$.

At this point $Q$ has its maximum value, $Q_{\max}$:

$$Q_{\max} = \frac{1}{\omega C_{\min} R_s}. \tag{8}$$

Where $f_c$ of Eq. (9) is called the cutoff frequency, which is an important factor for showing high frequency characteristics

$$f_c = \frac{1}{2\pi C_{\min} R_s}. \tag{9}$$

The condition of oscillation is given by Eq. (10)

$$\frac{C_1}{C_0} \geqq \frac{1}{Q_{\max}}. \tag{10}$$

Therefore $C_1/C_0$ and $Q_{\max}$ must be large for oscillation. First we will consider the condition necessary to increase the value of $C_1/C_0$. From Eq. (6), a large amplitude of $V_1$ is favorable for large $C_1/C_0$. However if we use too high a voltage for $V_1$, the instantaneously impressed voltage either extends into the forward region or become greater than the breakdown voltage, and the loss due to the barrier conductance increases excessively. Therefore to prevent excessive loses, the values of $V_1$ and $V_0$ cannot be selected independently each must be selected on the basis of the value of the other. Also, it is desirable for the ratio of $C_{\min}/C_c$ the denominator of Eq. (6) to be as small as possible in order to obtain a large ratio of $C_1/C_0$. Therefore it is important that the value of $C_{\min}$ be as small, and that the value of $C_c$ be as large as possible.

It is also necessary that $C_{\min}$ and $R_s$ be small for large $Q$. If it is assumed that the noise of diode comes mainly from the thermal noise of the equivalent resistive component, $C_B$ and $R_s$ must be small, for decreasing the noise coincides with the requirement of high $Q$. As $C_{\min}$, $R_s$ etc. are determined by manufacturing process of a diode, a superior process must be selected.

## 3. Measurement

The block-diagram of the measuring circuit is shown in Fig. 5. The impedance of the diode was measured using a coaxial type standing wave detector at 6 kMc. Barrier impedance was obtained from the measured value by subtracting holder capacitance,

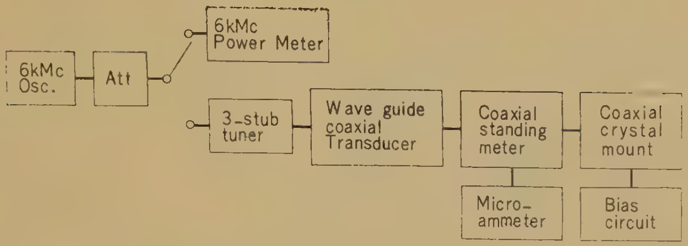


**Fig. 5**—Block diagram of measuring circuit.

spreading resistance, and whisker inductance which are also measured by the same detector. In the measurement forward and reverse biases voltage were applied to the diode. The breakdown voltage was defined as the reverse voltage at which reverse current was 100 $\mu$A.

## 4. The Result of Measurements

### 4.1. Variation of Barrier Capacitance with Bias Voltage

We measured several types of diodes. Small signal admittances of the 1N23B are shown in Fig. 6, and those of two silver bonded diodes are shown in Fig. 7. The voltage-current characteristics of the measured diodes are shown in Fig. 8. The silver bonded diode has larger forward conductance and much smaller reverse conductance than the other diodes. From Figs. 6 and 7, it is found that the barrier conductance and susceptance of the diodes increase with forward bias, and they become infinite at over +0.6 V. In the reverse bias region the conductance component becomes almost constant; and only the susceptance component, that is the barrier capacitance, varies. As the reverse bias voltage nears the breakdown voltage, the conductance component increases.

The variation of barrier capacitance $C_B$ vs. bias voltage is shown in Fig. 9; abscisa is the value of $(\phi - V_0)$, and the point marked 0 is the point of 0 bias. Then the right

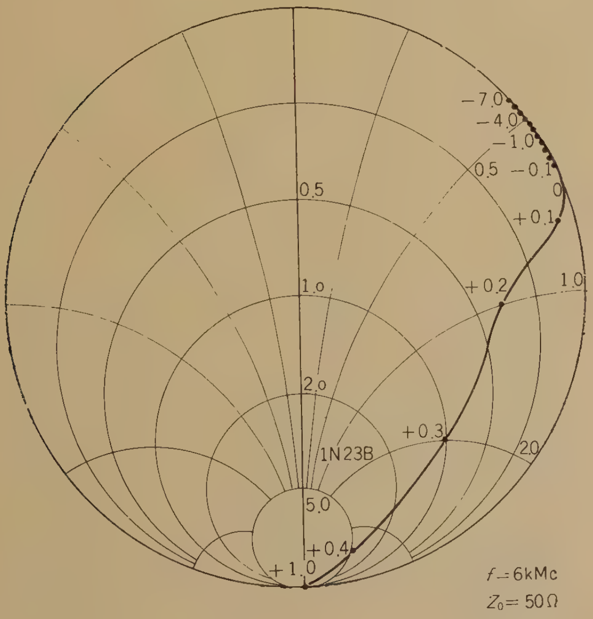


**Fig. 6**—Barrier admittance of 1N23B diode.

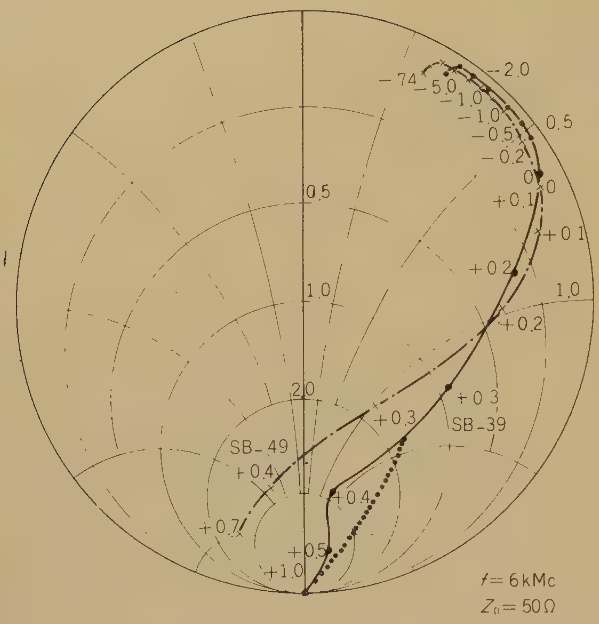


**Fig. 7**—Barrier admittance of silver bonded diodes.

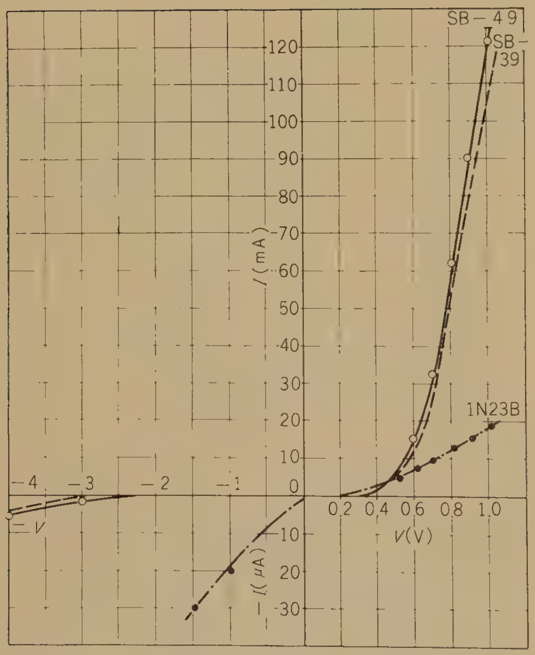


**Fig. 8**—Voltage-current characteristic of diodes.

side from 0 shows the reverse bias region and the left side shows the forward bias region. In the reverse bias voltage region, where the static capacitance of the point contact is not effective, the variation of the barrier capacitance agrees with the theoretical value, but in the forward bias region $C_B$ increases more steeply than theoretical value.

It is belived that this phenomenon is due to diffusion capacitance; it is known that a diffusion admittance occurs in the forward bias region and that the conductance component and the susceptance component of the diode become equal in the microwave region. Therefore the barrier forward admittance must follow the dotted line in Fig. 7. In addition it has been discovered by Kita that the barrier susceptance of such diodes becomes inductive in the forward bias region at microwave frequencies, as shown by the curve for diode SB-49 in Fig. 7, and it has been proven by Mr. Kanai that the phenomenon is due to conductivity modulation. Therefore it is considered that the curve of diode SB-39 obtained experimentally is the superposition of the diffusion admittance (i.e. dotted curve) and the inductive components.

Next, the curves of $C_B - C_{\min}$ vs. bias

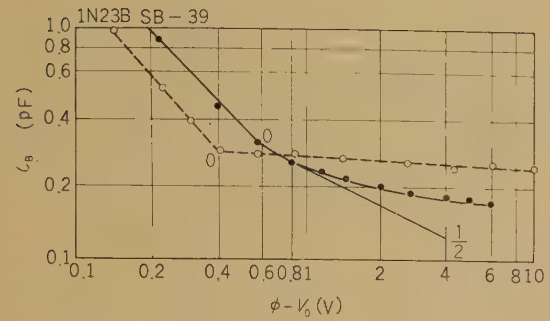


**Fig. 9**—Barrier Capacitance vs. $\phi - V_0$.

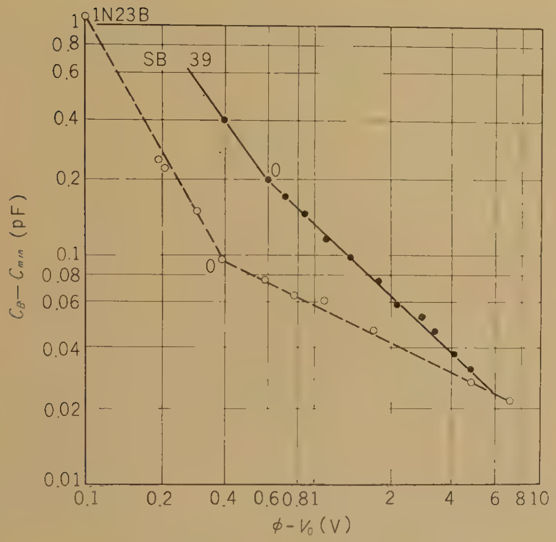


**Fig. 10**—$C_B - C_{\min}$ vs. $\phi - V_0$.

**Table 1**

DIODES CONSTANTS

| | $R_s$ (Ω) | $C_{min}$ (pF) | $C_{min}R_s$ (pF·Ω) | $f_c$ (kMc) | $C_1/C_0$ |
|---|---|---|---|---|---|
| Silver Bonded Diode | 5-10 | 0.1-0.2 | 0.32-0.6 | 150-300 | 0.8 |
| 1N23B | 36 | 0.25 | 9 | 18 | 0.02 |
| Point contact Germanium Diode | 36 | 0.15 | 5.4 | 29 | 0.02 |

voltage are shown in Fig. 10.

Variation of $C_B - C_{\min}$ is almost linear when plotted on log-log paper except near the breakdown voltage. This proves that the approximation of Eq. (2) is correct.

We obtained $R_s$, $C_{\min}$ and $C_c$ from the measurements, and they are shown in Table 1. $C_{\min}$ and $R_s$ of the silver bonded diode are smaller and $C_1/C_0$ is greater than those of other diodes. Therefore it is found that the silver bonded diode is most suitable for use as a parametric amplifier diode.

### 4.2. Effect of Electrical Forming on the Diode Characteristics

As previously mentioned our electrical forming has used capacitor discharge current. In this case forming voltage is increased step by step. By this electrical forming the voltage-current characteristics of the diode are changed as shown in Fig. 11; the forward resistance decreases, but the reverse characteristic is almost invariant and thus the overall characteristics are improved. In Fig. 11 the circled numbers represent the number of times the electrical forming current was applied, and 0 represents, the point contact without forming. We measured $R_s$, $C_{\min}$, and $C_c$; and the results are shown in Fig. 12. The abscisa is forward current at +1V. It is found that according to the number of times of electrical forming $R_s$ decreases, and that $C_{\min}$ does not increase until the forward current reaches 100 mA, but it increases abruptly when the forward current becomes larger than this value. Therefore $C_{\min}$ $R_s$ take minimum values at about 100 mA. Since $C_c$ increases with forward current, $C_{\min}/C_c$ decreases with forward current. As a results, we found the best electrical forming condition gives a diode in which forward current is 100 mA with a forward bias voltage of +1V.

### 5. Characteristics of the Parametric Amplifier

We made a 6 kMc parametric amplifier using a silver bonded diode. Pump frequency

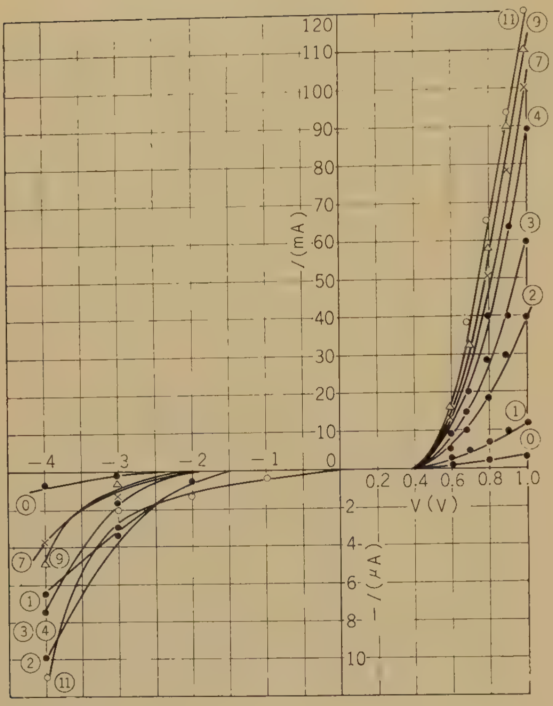


**Fig. 11**—Variation of voltage-current characteristics caused by electrical forming.

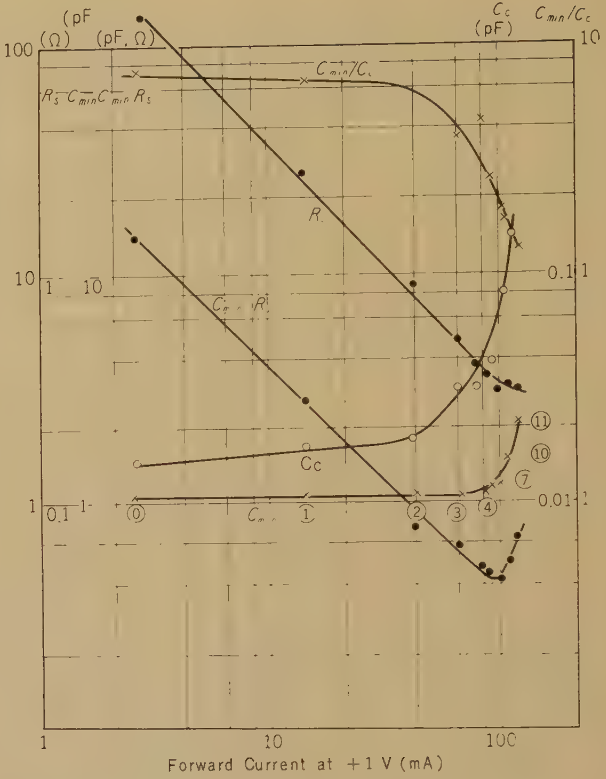


**Fig. 12**—Variation of diode characteristics caused by electrical forming.

was about 12 kMc and pump power was about 20 mW. The bandwidth was 40 Mc at 20 dB gain and the noise figure for single sideband was about 5 dB. It will be 2 dB for double sideband.

## Conclusion

It was found that the silver bonded diode has superior characteristics when used as a microwave parametric amplifier diode. We made a parametric amplifier using the silver bonded diode, and an amplifier with good characteristics was obtained. The authors wish to express their gratitude to Messrs. Nakamura, Someya, Masuda, Oguchi, Okajima, and Inage for their valuable help and suggestions during to this work.

## References

(1) S. Kita and T. Fujii, "Microwave Amplification by Use of Crystal Diode, *Annual Convention Report. I.E.C., of Japan,* Oct. 1954.
(2) S. Kita, "A Harmonic Generator by Use of the Nonlinear Capacitance of Germanium Diode," *Proc. I.R.E.*, 46, p. 1307, 1958.
(3) S. Shockley, "Electrons and Holes in Semiconductor," D. V. Norstrand, 1950.

* * * *

U.D.C. 621.923.75.001.2:534.133

# VHF Crystal Polishing and the Nature of Polished Quartz Surfaces*

**Ichiro IDA**† and **Yuzo ARAI**†

*The highest frequency of VHF crystal units in practical use produced by lapping is considered to be about 75 Mc/s; and this limit seems to be caused by vibration loss due to irregularities of the surface of the quartz. Therefore, in the first place, polishing techniques for finishing the surface to a high degree have been pursued with regard to the working methods, processes, and precise measurements of the mechanical quantities of quartz plates, which will lead to the establishment of a basis for making crystals with frequencies of up to 140 Mc/s with sufficient yield. In the second place, from our understanding of the deformation of thin polished plates, the nature of skin stress, stages of worked layers, and depths of mechanical disturbances have been explained. With the results thus obtained, the mechanism of polishing quartz that is explained as the aggregation of micro-scratchings by points of abrasives in the process of polishing is described. Further, a model of the polished layer, by which mechanical factors having influence on the vibration loss may be suggested, is shown.*

## Introduction

The practical frequency limit of VHF crystal units obtained by lapping is considered to be about 75 Mc/s. This is because the roughness and cracks left on lapped surface have a serious influence on the vibration loss of the crystal units, since the dimensions of these imperfections are not negligible compared with wave-length of the elastic wave in the higher frequency range. (1) The surface of quartz plates, therefore, must be finished to a high degree in order that crystal units having the desired properties may be produced in the high frequency range. Also, the plates are extremely thin and must be accurately parallel. These requirements mean that, in the polishing technique for a thin, brittle material such as quartz plate, some specific and difficult problems come to the front that do not arise in polishing of optical materials nor in mechanical lapping.

Although Twyman gave general working conditions for polishing quartz in optical workshops,(2) he did not touch on the appropriate method for thin plates whose thickness is as small as 35 $\mu$. On the other hand, several studies on the nature of polished quartz surfaces by electron diffraction, including Kamogawa's unique study,(3) have been made, but they were all concerned with the Beilby layer itself, so that its relation to working methods or conditions have not always been clear. Moreover, Gerber has already reported that the characteristics of crystal units obtained by polishing were excellent,(4) but he did not describe the details of how to work oscillator-plates nor deal with the mechanism of polishing quartz.

In this paper, with the development of a polishing technique for very thin quartz plates whose frequency is up to 140 Mc/s, the nature of polished layers of quartz is studied from the standpoint of residual stress and deformation of the quartz plates.

---

* MS in Japanese received by the Electrical Communication Laboratory, Jan. 30, 1960. Originally published in the *Kenkyû Zituyôka Hôkoku* (*Electrical Communication Laboratory Technical Journal,*) Vol. 9, No. 3, pp. 245–317, 1960.

† Precision Research Section.

## 1. Polishing of VHF Crystal Units

In this chapter, working method, process, and measurements of mechanical quantities of quartz plates are described ; and the experimental results are discussed from the viewpoint of working accuracy in connection with the polishing of about three hundred plates, whose thickness ranged from 0.035 to 0.15 mm.

### 1.1. Working Method

#### 1.1.1. Problems in Polishing

By polishing, the surface can be mirror-finished with the roughness and cracks originating in lapping, which cause a great number of concoidal fractures to brittle materials, removed. Also, the mechanism of polishing is discussed from various points in view ; which include : micro-cutting ; plastic flow ; chemical reaction, especially hydrolysis ; melting ; etc. Therefore, the principle of a lapping machine, in which the working accuracy depends upon geometric elements and kinematic conditions, can not be applied to polishing. That is to say:

(1) It is indispensable for obtaining accuracy to make the ratio of the diameter of the lap to that of the work greater than a certain definite value ; but when used on a pitch polisher the value of this ratio is limited by difficulties in forming and trueing the lap.

(2) Though the resultant rotatory motion including spinning will ensure the accuracy of plane lapping as already described,⁽⁵⁾ it is necessary in this case for the work to be supported in a free state. Since, in polishing, the resistance between both contact surfaces becomes large, the work will be broken if it is supported freely, and the thinner the plate, the severer the breaking will be.

(3) In the case of free support of the work, low trueing ability of the polishing abrasives makes the polishing of only the peripheries of the work's surface possible ; and this will be accelerated by light loads.

(4) If a solid polisher is used, origination of scratches will be unavoidable, thus resulting in a marked reduction of the polishing effect. By the use of a synthetic plastic lap, the application of plane parallel lapping will be possible to a certain degree ; in which case, however, the finish and accuracy obtained will be insufficient.

(5) In addition to the problems mentioned above, thickness of plates may be as small as 1/140 to 1/400 of their diameter. Moreover, accuracy must be of the order of 0.1 $\mu$. Thus, the conditions for making thin oscillator-plates are very severe.

As seen from these problems, the first consideration in the development of the working method for quartz plates by polishing instead of lapping should be the study of a working machine, methods, and process.

#### 1.1.2. Motion of a Lens Polishing Machine

In an analytical treatment of the motion of a lens polishing machine including reciprocation, coordinates are determined as shown in Fig. 1, and the motion at any point on the work is observed. The motion is composed of reciprocation of a lever, rotation of a block around a post and relative revolution of a pitch polisher. Therefore, the locus on a pitch polisher for any point on the work is determined by the rotation of the fixed coordinates of the crank and the lever to the rotatory coordinates of the pitch polisher. Thus the position of point $V$ is expressed by

$$x'_V = -R(\dot{\phi}-\omega_3)\sin(\varepsilon+\eta-\tau)$$

$$+r(\omega_2-\omega_3)\sin(\delta+\eta-\tau)$$

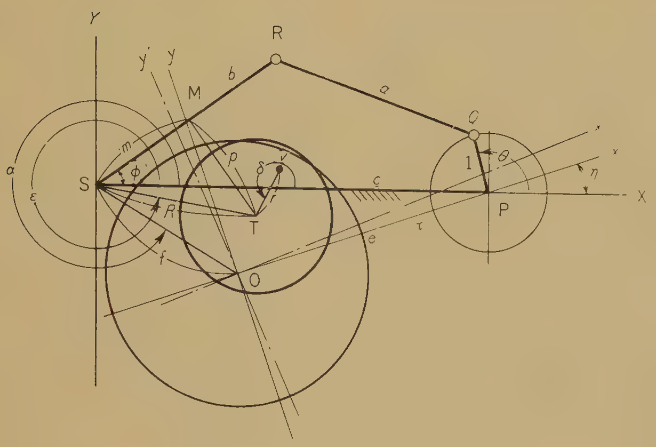
$$-f\omega_3\sin(\alpha+\eta-\tau)$$

$$y'_V = -R(\dot{\phi}-\omega_3)\cos(\varepsilon+\eta-\tau)$$

$$+r(\omega_2-\omega_3)\cos(\delta+\eta-\tau)$$

$$-f\omega_3\cos(\alpha+\eta-\tau),$$

where $\dot{\phi}$ is the angular velocity of the



O : Center of Pitch Polisher
P : Center of Crank Disc
Q : Connecting Point between Connecting rod and Crank
R : Connecting Point between Lever and Connecting Rod
S : Center of Revolution of Lever
M : Supporting Point of Arm on Lever
T : Position of Post
V : Any Point on Work
1 : Radius of Crank
$a$ : Length of Connecting Rod
$b$ : Length of Lever
$c$ : Length of Fixed Link
$e$ : Distance between Pitch Polisner and Crank Disc
$\theta$ : Revolution Angle of Crank
$\phi$ : Revolution Angle of Lever
$\varepsilon$ : Revolution Angle of ST about XSY Co-ordinates
$\delta$ : Revolution Angle of Point V about XSY Co-ordinates
$\alpha$ : Angular Position of OS about XSY Co-ordinates
$\tau$ : Revolution Angle of Pitch Polisher about Fixed Co-ordinates
$\eta$ : Angle between xO and XS
$f$ : Distance between Pitch Polisher and Center of Lever
$m$ : Length of Arm on Lever
$p$ : Distance of Post on Arm
$R$ : Distance between Center of Lever and Post
$r$ : Distance of any Point on Work from Center of Post

**Fig. 1**—Motion of a lens polishing machine.

lever,* $\omega_2$ that of the block, and $\omega_3$ that of the pitch polisher.

Elimination of $t$ from the above two equations leads to the locus, and by composition of $\dot{x}'_V$ and $\dot{y}'_V$, the resultant velocity of the point is obtained as follows:

$$U^2=R^2(\dot{\phi}-\omega_3)+r^2(\omega_2-\omega_3)^2+f^2\omega_3^2$$

$$-2Rr(\dot{\phi}-\omega_3)(\omega_2-\omega_3)\cos(\delta-\varepsilon)$$

$$+2Rf(\dot{\phi}-\omega_3)\omega_3\cos(\alpha-\varepsilon)$$

$$-2rf(\omega_2-\omega_3)\omega_3\cos(\delta-\alpha)$$

As seen from these equations, the tracing of the curve is not easy, and besides, if the working condition, for instance the crank's radius changes, (Fig. 1) all the other conditions will vary too. This suggests that the numerical calculation has little meaning. Moreover, the above analysis was made on the assumption that no deformation occurred, despite the fact that it occurred every moment in polishing. From these considerations, the treatment of the motion of the polishing machine should be experimental, and then the main part of motion is assigned to reciprocation because of its being nearly equal for all positions, even if it varies with time. In addition, revolution is given to the pitch polisher with a speed lower than that of the crank with a view to compensating for the radial inequality which would arise if only revolution were given.

---

* $\phi=\omega_1\left(\frac{1-c\cos\omega_1 t}{1+c^2+2c\cos\omega_1 t}+\frac{c\sin\omega_1 t\{c+(1+b^2+c^2-a^2+2c\cos\omega_1 t)/(1+c_2+2c\cos\omega_1 t)\}}{\sqrt{4b^2(1+c^2+2c\cos\omega_1 t)-\{(1+c^2+b^2+a^2)+2c\cos\omega_1 t\}^2}}\right)$

where $\omega_1$ is the angular velocity of a crank.

Consequently, in this study, the standard speed is fixed at 9.5 rpm for the main axis for the pitch polisher and at 40 rpm for the crank ; while the standard amplitude is arranged to be 60 mm on the post attached to the arm.

### 1.1.3. Polishing Process

Plates to be polished are *AT* cut round crystals of 0.035 to 0.15 mm in thickness and 14 mm in diameter, and these must be worked precisely to the order of 0.1 $\mu$ and with a mirror-finish of the order of 0.01 $\mu$. Fig. 2 illustrates the polishing process, with the main process shown in thick black lines. Generally speaking, the process consists of lapping as a preliminary step, polishing to give a mirror-finish, and optical contact for fixing plates with high precision ; including measurements of such mechanical quantities as parallelism, flatness, and roughness.

As described later, if thinly lapped plates are polished on a single side, they will be deformed concavely on the polished side, because of the extremely large compressive stress on the lapped surface.* Then, the thickness of plates before the final polishing is determined to be about 0.6 mm, with roughness given by hand lapping with elutriated AO Emery No. 304 being about 0.5 $\mu$. At this time, 37 plates fixed to a block with pitch or paraffin are simultaneously worked. Parallelism♯‡ must be within 0.03 mm, while it is necessary for flatness to be within 0.5 $\mu$ for the diameter of 110 mm over which the crystals are arranged, assuming that the upper surfaces and the lower surfaces of these crystals comprise one continuous surface. For polishing, abrasives of cerium oxide are mixed with water and become pasty. They are supplied to the pitch polisher, on which hexagonal meshes are serrated, at intervals of 5 to 10 minutes. The polishing pressure ranges from 10 to 40 g/cm$^2$. As shown in Fig. 3, the pitch polisher is located beneath the work in the case of a cemented holder, while it is located on the work in the case of an optical flat holder.

### 1.1.4. Optical Contact Method

If a quartz plate has poor parallelism, especially if it is wedge-shaped, vibration activity will be lowered. Therefore, the application of cement generally used for such working will be impossible in the final polishing process due to cementing errors, cementing strains, dimension change etc.. For this reason, the optical contact method,(6) which is said to make both precise surfaces closely contact each other through diffused water films, should be applied. In view of the very small thickness of the plates and the simultaneous fixing for many plates, the following method is adopted here in practice :

(1) In consideration of the attaching strength and the cementing strain which is likely to occur, the thickness of a plate in optical contact is determined to be about 0.6 mm with flatness of about 0.1 $\mu$, while the flatness of the optical flat to be contacted to plates is within 0.3 $\mu$ over the effective diameter of 120 or 130 mm. These samples

---

* The reason for this phenomenon will be discussed in Chapter 2.

‡ Pallalelism♯, in this paper, refers to the difference between the maximum thickness and the minimum thickness of the thickest and the thickness crystals being worked.

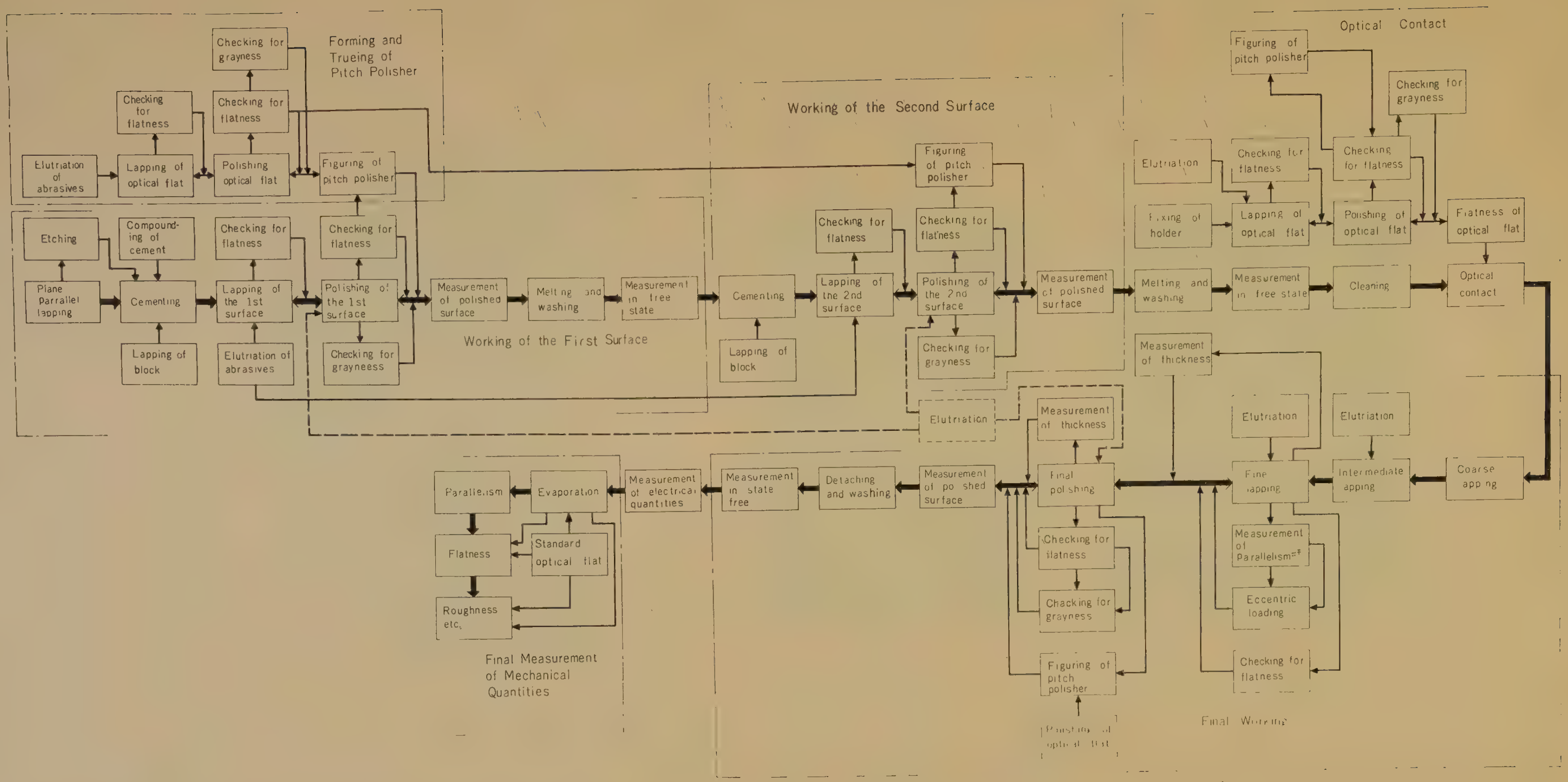
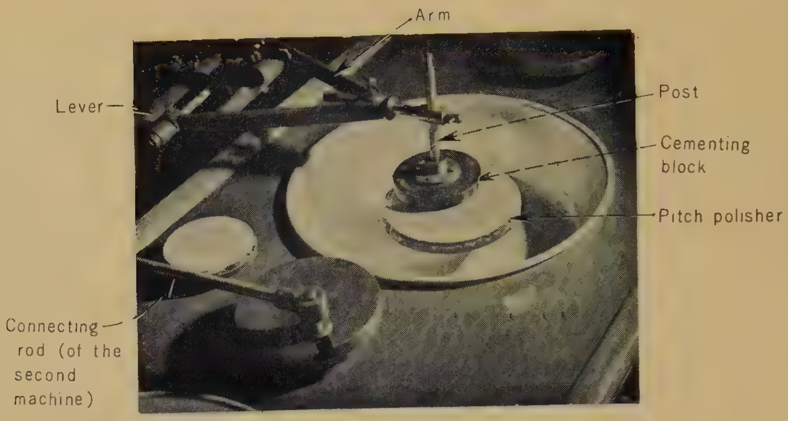
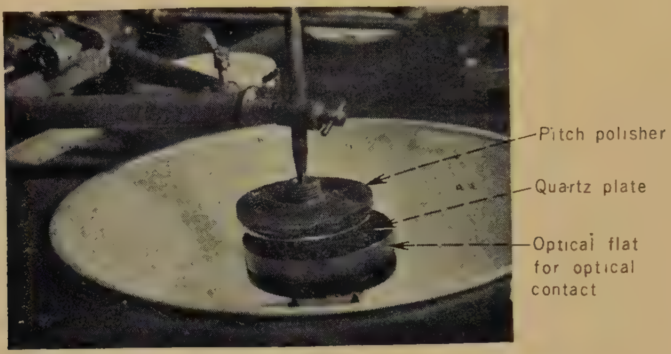


**Fig. 2**—Polishing process.

‡ Refer to the footnote on page 122.

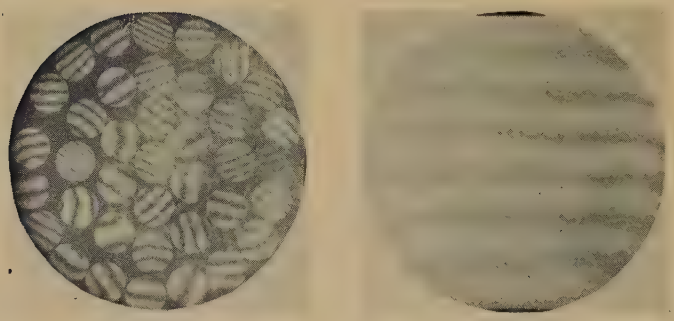


(a) In the Case of a Cementing Block Holder



(b) In the Case of an Optical Flat Holder.

**Fig. 3**—State of polishing.



t: 0.9 mm

Diameter: 120 mm.

(a) Quartz Plates (Experiment V) in the Free State.

(b) Optical Flat Surface (Experiment III)

Fringe Interval ≒0.3 μ

**Fig. 4**—Interference fringes showing flatness of surfaces to be optically contacted.

are photographed in Fig. 4.

(2) After polishing, crystal plates and optical flat are immersed in a solution of potassium dichromic acid dissolved in water for 24 hours, and then washed with distilled water and ethyl alchohol. In effecting contact, pure or distilled water is made to run out to make both surfaces touch in a wet state so as to bring about Newton's one colour by making use of a bamboo tweezers.

(3) After both plates and the optical flat have been kept in a deccicator for 5 to 24 hours, the peripheries of the quartz plates are covered with a water-proof compound and then left again in the deccicator for 24 hours.

For the water-proof treatment, three methods as shown in Fig. 5 were tried, of which the one illustrated in the same Figure, (d) was found to produce the best result. In this method, a minute annular step with a depth of about 0.3 $\mu$ and a width of about 2 mm is etched by a saturated solution of ammonium bifluoide in water for 10 minutes, and then paraffin is melted into this part at about 80° C. As a result, whatever the thickness of plate may be, the protected area is wide enough to give a complete protection against water immersion.

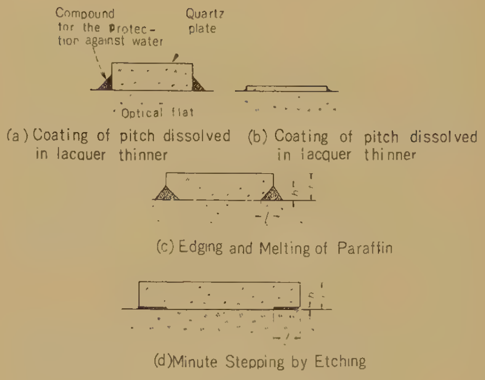

Compound for the protection against water
Quartz plate
Optical flat
(a) Coating of pitch dissolved in lacquer thinner
(b) Coating of pitch dissolved in lacquer thinner
(c) Edging and Melting of Paraffin
(d) Minute Stepping by Etching

**Fig. 5**—Methods of protection against water in optical contact.

(4) In detaching the plate from optical contact after completion of polishing, a safety razor blade is inserted under the side of the plate, making it deform elastically.

After accomplishment of optical contact, final lapping is continued until the thickness of plates becomes thicker than the desired value by about 2 $\mu$ ; also taking care to measure and correct for errors in parallelism,#‡ as will be described in the next paragraph.

### 1.1.5. Adjustment of Parallelism#‡ by Eccentric Loading

For one-sided working or single surfacing,

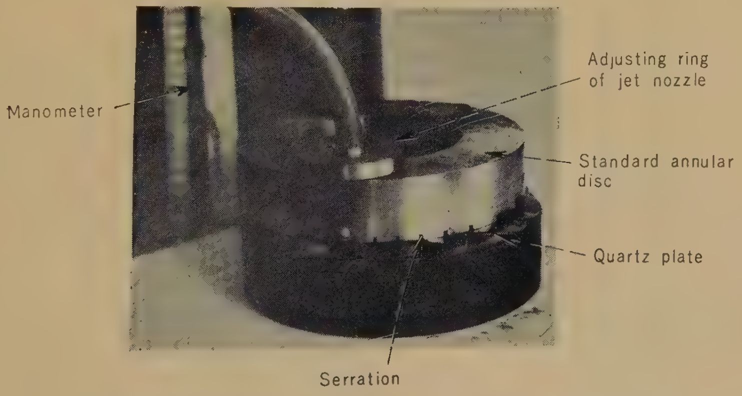


**Fig. 6**—Measuring apparatus for parallelism#‡ of plates.

---

‡ Refer to the footnote on page 122.

measurements of parallelism#‡ and adjustments based on the results of the measurements are necessary not to produce wedge-shaped plates. A standard annular disc equipped with the jet nozzle of a pneumatic micrometer, whose magnification is 11,000, is placed on the work surface ; and measurements on the peripheries of the plates are made after working the platesfor periods of five to ten minutes. In Fig. 6, its appearance is shown.

Thus, the highest position is worked, with an eccentric load given. In this case, in order to cause no kink on the worked surface, the following conditions will come to be necessary, if the pressure increases proportionally to the distance $(x, y)$ from the center O as shown in Fig. 7. That is to say:

$$a \leqq r/4,\ ^{(7)}$$

$$l \leqq \frac{W+Wa}{4Wa} \cdot r.$$

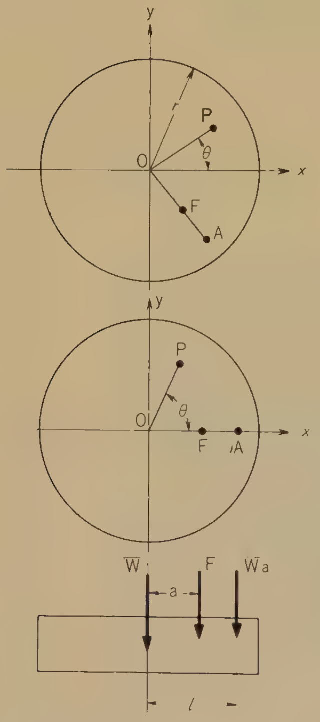


Fig. 7—Application of eccentric loading (Rumsay).

Moreover, $l$ is selected so as to be maximum under the following conditions in order to obtain the maximum efficiency ; That is,

$$Wa \leqq W/3,$$

where $W$ is the weight of the block fixing the crystal plates, $Wa$ the weight of the eccentric load, $a$ the distance of action of resultant force and $r$ the radius of the block. These values used are given in Table 1.

**Table 1**

CONDITIONS FOR ECCENTRIC LOADING

| $W$ kg | 1.092 | | 1.360 | |
|---|---|---|---|---|
| $W_a$ kg / $a/r$, $R$ | 0.204 | 0.293 | 0.345 | 0.425 |
| $a/R$ | 0.107 | 0.153 | 0.159 | 0.173 |
| $R$ | 2.5 | 4.1 | 4.5 | 5.6 |

Where $R$ is the ratio.
maximum pressure/minimum pressure.

During this adjustment, flatness for the diameter of 110 mm must be maintained within 0.5 $\mu$, the reason being to be described in the next section.

### 1.2. Measurements of the Mechanical Quantities of Quartz Plates

Roughly speaking, this measurement work is composed of the measurements of the mechanical accuracies of the plates during working, measurements of the plate thickness during final polishing, the measurement of mechanical quantities of the crystal plates such as paralleism, and flatness after completion ; also the inspection of surface quality both during working and after completion.

---

‡ Refer to the footnote on page 122.

### 1.2.1. Flatness Measurement During Polishing

Geometrical causes for the plates' having thickness variation may be classified into (1) error of parallelism[‡] over plates fixed, (2) wedge caused by error of flatness of polished surface and (3) wedge caused by an error in the flatness of the optically contacted surface.

The paralleism of a quartz plate, $\Delta t$, is expressed by the following equation.

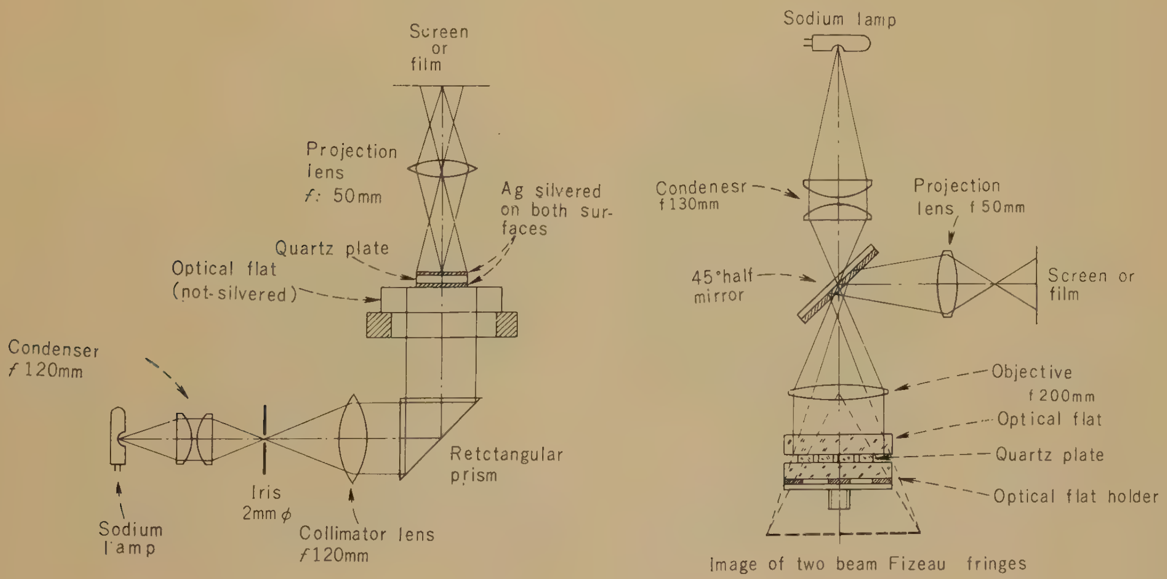
$$\Delta t = (a\lambda/4R)(m+4N).$$

where $R$ mm is the effective radius of the optical flat used to hold the crystals, $a$ mm the diameter of each crystal, $\lambda$ $\mu$ the wavelength of the light used, $m$ the number of fringes arising from cause (1), and $N$ the number of Newton's rings arising from causes (2) and (3).

As seen from the above equation, poor flatness has a serious influence on the variation of thickness of the plate, so that a value of flatness within $0.5\,\mu$ for entire working area will be necessary in the final lapping stage.

Fig. 8 (b) shows the optical path of a two beam interferometer, whereby the whole surface with a diameter of 120 mm can be recorded. Quartz plates of Fig. 9 (a) have been almost completely polished with flat surfaces, while those shown in Fig. 9 (b) still have grayness with edges "turned down."

As polishing continues, a pitch polisher becomes deformed and gradually wears out; and the degree of such deformation will be accelerated, unless trueing is applied. Generally speaking, this trueing work is a laborious job, because it is done by heating, forming, rubbing etc.. Therefore, with a view to improving this procedure, polishing of plates by one machine, and trueing of a slightly de-



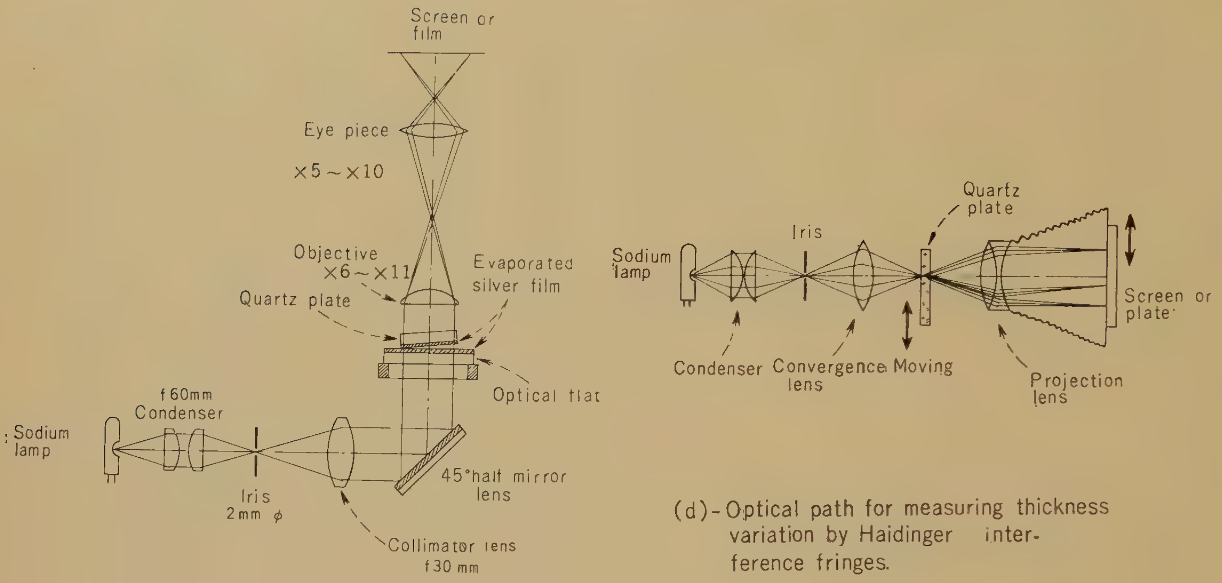
(a) - Optical Path for measuring Paralleilsm by Multiple Beam Fizeau Fringes.

(b) - Optical Path for measuring Flatness by Two Beam Fizeau Fringes.

**Fig. 8 (a)** and **(b)**—Optical arrangements of interferometers used for measurements of mechanical quantities of quartz plates.

---

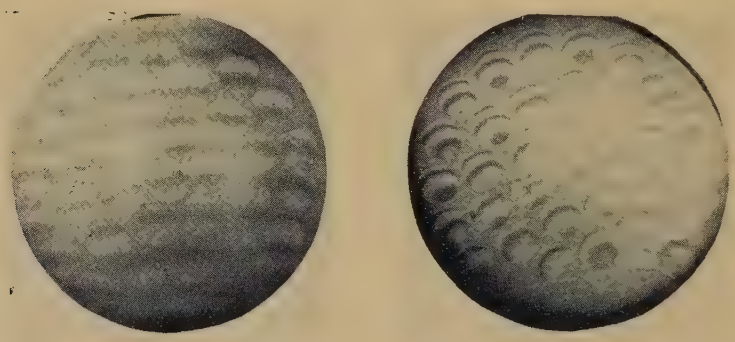
[‡] Refer to the footnote on page 122.



(c)-Optical path for measuring roughness by multiple beam Fizeau fringes.

(d)-Optical path for measuring thickness variation by Haidinger interference fringes.

**Fig. 8 (c)** and **(d)**—Optical arrangements of interferometers used for measurements of mechanical quantities of quartz plates.



(a) Almost Polished, in Experiment III, no Detachment, t 0.134 mm.

(b) Grayness Still Remains, in Experiment V, t 0.092 mm.

**Fig 9**—Examples of finally polished surfaces of quarty plates.

formed pitch polisher on an optical flat by another are performed simultaneously. This makes the reproduction of flatness easier, together with shortening the working time. The outline of this method is illustrated in Fig. 10.

### 1.2.2. Measurements of the Mechanical Quantities of Quartz Plates

In effecting the measurements of parallelism, flatness and roughness of quartz plates, silver is evaporated on to the surfaces of

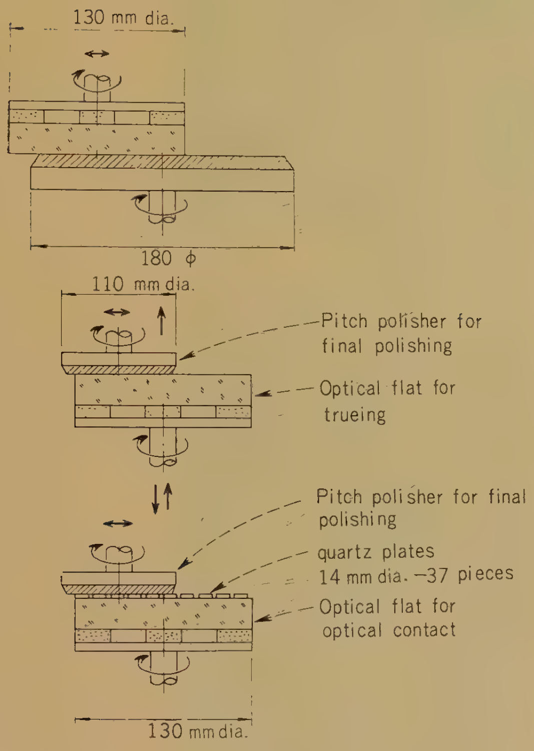

130 mm dia.
180 ϕ
110 mm dia.
Pitch polisher for final polishing
Optical flat for trueing
Pitch polisher for final polishing
quartz plates
14 mm dia. —37 pieces
Optical flat for optical contact
130 mm dia.

**Fig. 10**—Trueing of flatness by polishing with an optical flat.

the quartz and the optical flat at a vacuum of $(1 \text{ to } 1.5)\times 10^{-4}$ mmHg, and multiple beam(8) Fizeau fringes are produced between both surfaces of the quartz plate (parallelism) and between the surfaces of quartz and optical flat (flatness and roughness). For excellent parallelism that cannot be resolved by Fizeau fringes, thickness variation along the diameter of the plate is obtained by Haidinger fringes.

For roughness, a metallurgical microscope is used. Optical arrangements used in these measurements are illustrated in Figs. 8 (a), (c) and (d).

Samples measured by microgeometric fringes are shown in Fig. 11. The most noteworthy fact is that the local variation of thickness occures in a plate cemented to a block as shown in Fig. 12.

### 1.2.3. Inspection of Surface Quality

During polishing, a dark field reflection microscope with a magnification of 200 to 400 is used to inspect for the existence of grayness or scratches ; examples of which are photographed in Fig. 13.

After completion, a Schlieren microscope in transmission, whose optical arrangement is shown in Fig. 14, is used with a magnification of 90 to 165. This apparatus chiefly consists of a metallurgical microscope and the objective lens of an auto-collimator.

### 1.2.4. Measurement of Final Thickness of Crystal Plates in Contact with Optical Flat Holder

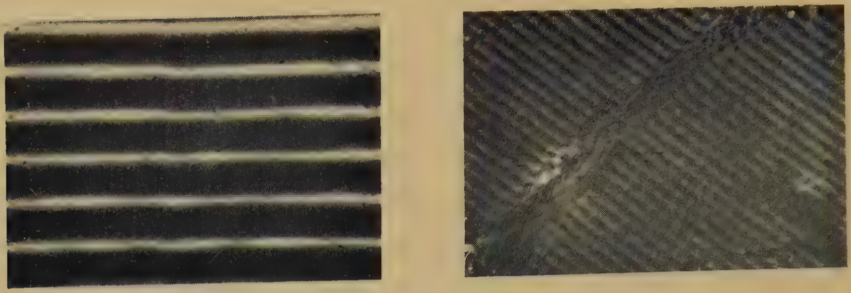
Thickness of a plate in optical contact with an optical flat is measured by a pneumatic micrometer to a extremely high degree of accuracy (of approximately $0.5\,\mu$) by comparison with block gages. However, if the interference method is applicable, the measurements will become more precise. For this reason, an interferometer with stepped reference surfaces has been made for trial.

This apparatus consists of the optical arrangements as shown in Fig. 15, in which two block gages of known thicknesses are wrung in to a single reference surface. The difference in thickness between these gages is compared with the height (thickness) between the upper surface of a quartz plate (polished) and the optical flat's surface. As shown in the lower part of the same Figure, two zero order fringes, which are produced by the measured surfaces and the stepped images which are produced by a beam splitter, appear in the field of the low-power microscope. Between the zero order fringes, some fringes may be counted in the following relation, that is to say:

$$T = t_0 \pm [S \pm \Delta S]$$

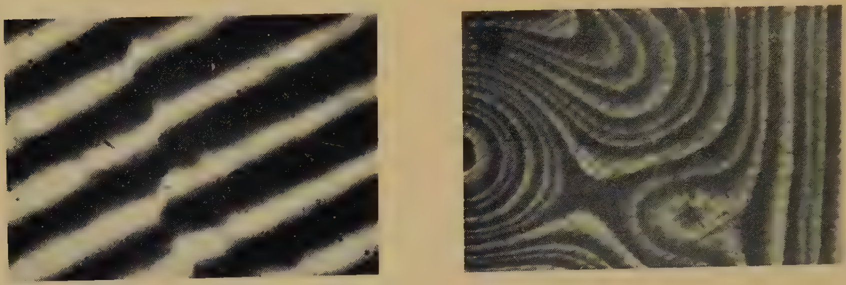
$$= t_0 \pm (\lambda/2)[N \pm n],$$

where $T$ is the thickness of a plate to be measured ; $t_0$ the difference in thickness



(a) Polished Surface (×55)

(b) Scratch (× 55)



(c) Crack (×30)

(d) Local Variaitons of Thickness Caused by the Use of Cement (Double Fringes due to Double Refraction) (×30)

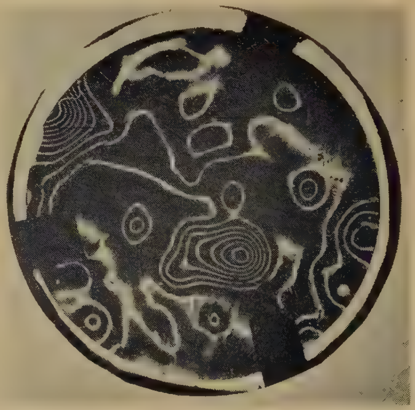
**Fig. 11**—Microgeometric interference fringes on quartz surfaces.

between the two block gages, which is known ; λ wave-length of the light used ; $N$ the number of fringes between the two zero order fringes, and $n$ the fraction of an order.

The above relation means that the thickness of a plate which is much larger than wave-length itself may be measured easily and accurately without fringe counting or preparation of a very thin reference body. The appearance of this interferometer is shown in Fig. 16.

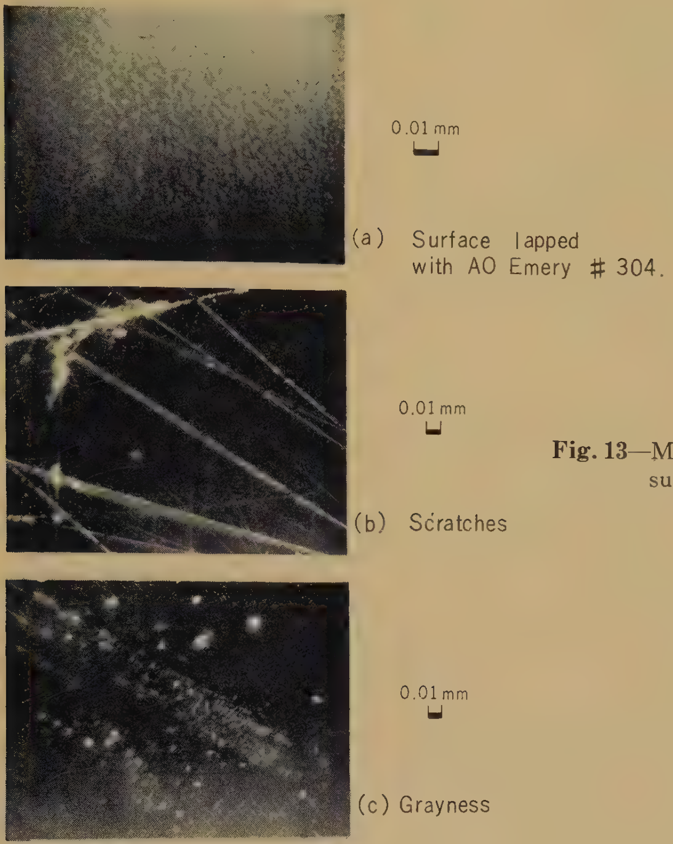
### 1.3. Polishing of 60–140 Mc Crystal Units

In order to meet the purpose of obtaining AT cut crystal units with frequencies as high as possible, nine experiments were performed and the results of these experiments are summarized in Table 2.



$t$: 0.182 mm, Not Vibrated

**Fig. 12**—Macrogeometric multiple beam interference Fizeau fringes indicating the local variations of thickness of a quartz plate caused by the breakage of optical contact.



(a) Surface lapped with AO Emery # 304.

(b) Scratches

(c) Grayness

**Fig. 13**—Microphotographs of quartz surfaces in the dark field.

### 1.3.1. Parallelism#‡ during Final Lapping

Parallelism#‡ converges to within 1 $\mu$ as shown in a few examples in Fig. 17. The net lapping time required for obtaining parallelism#‡ of this order covered a relatively wide range from 30 to 250 minutes, and it was not always proportional to the number of times of adjustment which ranged from 7 to 28. This is of course due to the overload, and is also dependent on the flatness of the whole lapped surface.

### 1.3.2. Flatness of the Surface Optically Contacted

Plates optically contacted have a thickness of 0.6–2.2 mm and their flatness are all

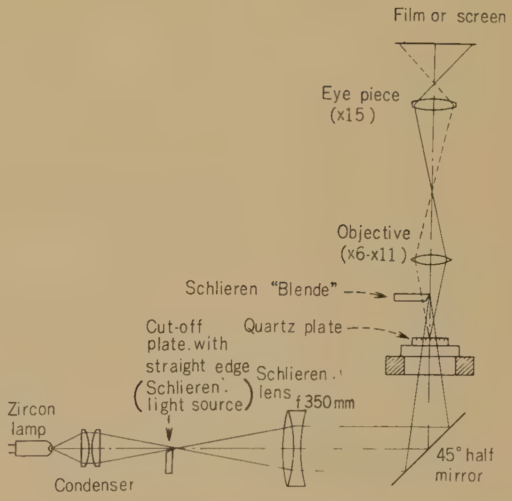


**Fig. 14**—Optical arrangement of Schlieren microscope.

---

‡ Refer to the footnote on page 122.

**Table**

### TOTAL RESULTS OF POLISHING

| Number of Experiment | | I | II | III |
|---|---|---|---|---|
| Initial Thickness, mm | | 2. 5 | 2. 3 | 0. 7 |
| Number of Plates Worked Simultaneously | | 3. 1 | 31+6[1] | 31+6 |
| Working Time until Attainment of Optical Contact | 1[2] | – | – | 11 |
| | 2 | – | – | 15 |
| | 3 | – | – | 17 |
| | 4 | – | – | |
| | Total | – | – | 43 |
| Polishing Position before Optical Contact | | Upper[3] | Lower[4] | Lower |
| Thickness when in Optical Contact | | 2. 2 | 2. 1 | 0. 6 |
| Diameter of Optical Flat above | | 120 | 120 | 120 |
| Flatness of Optical Flat above | | +[5]0. 15 | +0. 3 | −0. 1 |
| Days Necessary for Flatness above | | 40 | 30 | 20 |
| Time in the Deccicator after Optical Contact, Hours | | 5 | 5 | 5 |
| Lapping Time after Optical Contact, Hour | | – | – | 4 |
| Thickness of plate at Commencement of Adjusting Parallelism,#‡ mm | | – | – | 0. 155 |
| Aggregated Times of Working and Measurement after Adjusting Parallelism#‡; Hour | | – | – | 3 |
| Adjusting Number | | 20 | 12 | 7 |
| Parallelism#‡, μ | | 0. 3 | 1. 0 | 0. 2 |
| Polishing Position in Final Polishing | | Lower | Lower | Lower |
| Kind of Pitch | | No. 4 | No. 3 | No. 2 |
| Figuring Method of Pitch Polisher | | H[6] | H | M[7] |
| Final Polishing Time, Hours | | – | – | 17 |
| Flatness of Finally Polished Surface, μ | | +3. 3 | +0. 6 | +0. 15 |
| Final Thickness of Plate, mm | | 0. 125 | 0. 148 | 0. 134 |
| the Best Parallelism Obtained, μ | | <0. 2 | <0. 1 | 0. 2 |
| the Best Flatness Obtained, μ | | 0. 3 | <0. 1 | 0. 2 |
| the Highest Frequency Obtained, Mc-Order | | 66-the 5th | 79-the 7th | 87-the 7th |
| the Lowest Series Arm Resistance,[8] Ω | | 29 | 40 | 34 |

Note: 1) Number of Dammi. 2) Number of faces polished. Number of the repetition over two means repetitions.

‡ Refer to the footnote on page 122.

2

VHF CRYSTALS PLATES

| IV | V | VI | VII | VIII | XI |
|---|---|---|---|---|---|
| 0.7 | 1.0 | 1.5 | 1.2 | 1.2 | 1.2 |
| 37 | 37 | 31 | 19 | 37 | 37 |
| 16 | 13 | 15～20 by removal of grayness with flatness of within 0.3 μ | | | |
| 15.5 | 14 | | | | |
| / | / | | | | |
| / | / | | | | |
| 31.5 | 27 | 30～40 | | | |
| Lower | Lower | Upper | Upper | Upper | Upper |
| 0.6 | 0.9 | 1.2 | 1.0 | 1.0 | 1.0 |
| 130 | 130 | 130 | 120 | 120 | 130 |
| −0.07 | −0.08 | <0.1 | <0.1 | <0.1 | <0.1 |
| 10 | 1/8 | – | – | – | – |
| 5.5 | 24 | 2～3 by slow-cooling in the furnace | | | |
| 6 | 6 | – | – | – | – |
| 0.150 | 0.170 | 0.18 | 0.16 | 0.10 | 0.06 |
| 6 | 12 | – | – | – | – |
| 28 | 19 | 19 | 12 | 18 | 7 |
| 0.2 | 0.4 | 0.2 | 0.1 | 0.2 | 0.2 |
| Lower | Lower | Lower | Lower | Lower | Lower |
| No. 3 | No. 3 | No. 3 | No. 2 | No. 2 | No. 3 |
| M | M | H | H | H | H |
| 16 | 8.3 | 10 | 16 | 9 | 20 |
| +0.18 | +0.15 | +1.8 | +1.0 | +1.5 | −0.3 |
| 0.090 | 0.092 | 0.0782 | 0.0963 | 0.066 | 0.035 |
| 0.5 | 0.2 | 0.2 | 0.2 | 0.3 | <0.1 |
| 0.5 | 0.3 | not measured | | | |
| 92-the 5th | 90-the 5th | 105-the 5th | 120-the 7th | 125-the 5th | 140-the 3th |
| 26 | 25 | 30_ | 50_ | 40_ | 10 |

3) Work was positioned on a pitch polisher. 4) A pitch polisher was positioned on work. 5) + convex, − concave. 6) Trueing by Forming. 7) Trueing by Polishing with an Optical Flat. 8) At the highest frequency.

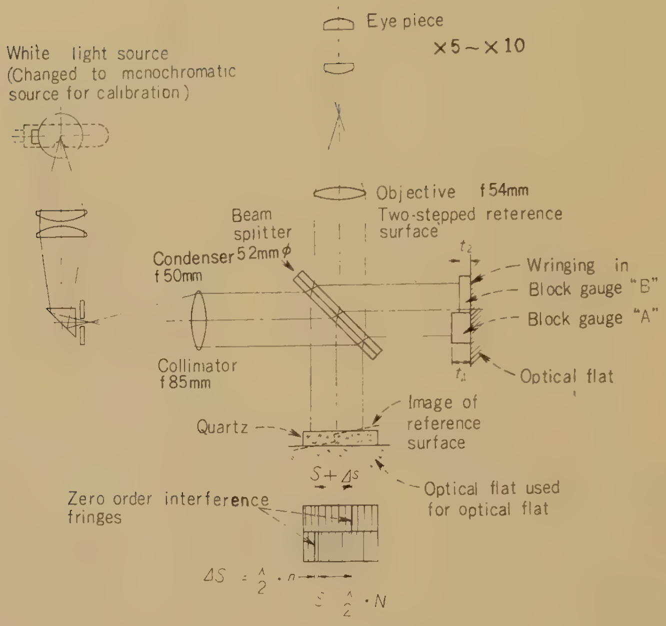


Fig. 15—Optical arrangement of the interferometer with stepped reference surfaces.

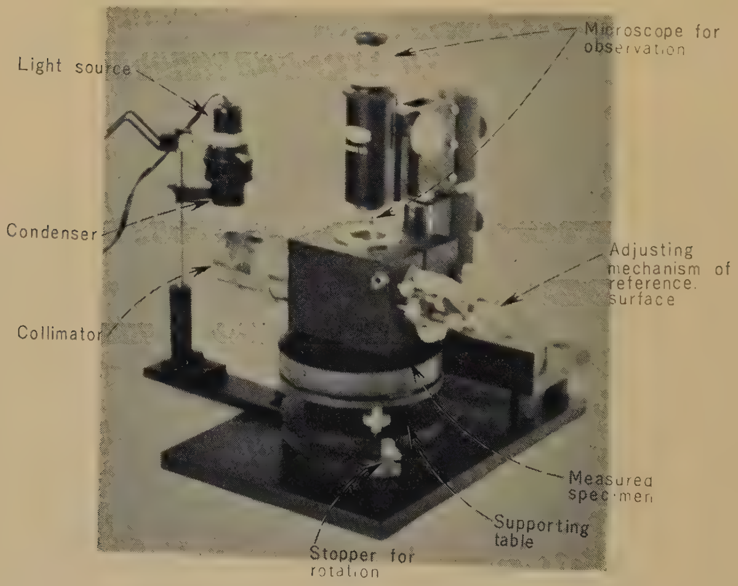


Fig. 16—Interferometer for measuring thickness of quartz plate in the case of optical contact.

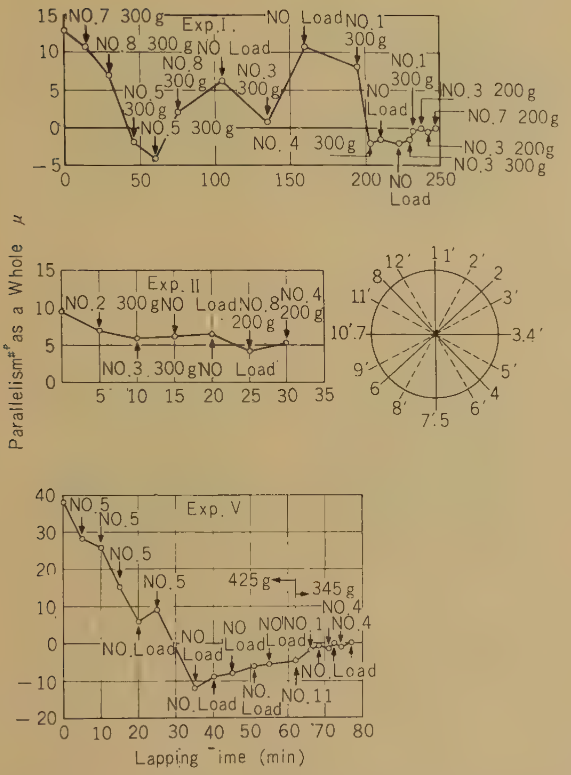


**Fig. 17**—Convergence of parallelism#‡ of quartz plates by eccentric loadings.

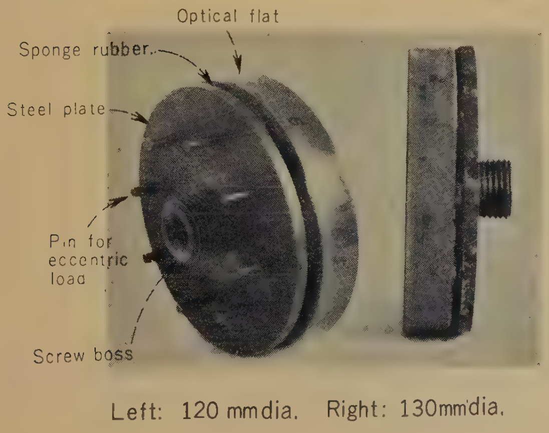


**Fig. 18**—Optical flats for "optical contact" and their holders.

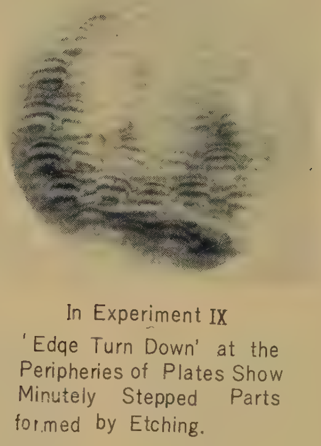

In Experiment IX
'Edge Turn Down' at the Peripheries of Plates Show Minutely Stepped Parts formed by Etching.

**Fig. 19**—The finally polished surface of quartz plates shown by interference fringes.

within 0.1 μ (refer to Fig. 4). By uniform thermal dissipation through scattered pieces of sponge rubber, flatness of within 0.3 μ may be ensured for an optical flat, whose appearance is shown in Fig. 18.

### 1.3.3. Flatness of the Finally Polished Surface

The flatness of the finally polished surface is of course affected by that of the finally lapped surface ; but it is also influenced by the degree of removal of grayness and the thickness of the water-proof compound. In the case of a plate with the thickness of 0.035 mm as shown in Fig. 19, flatness is good and parallelism#‡ is also excellent owing to the complete polishing to be accomplished by the effect of minute stepping. On the contrary, plates shown in Fig. 9 (b) represent bad flatness, with grayness indicated as a result of the incomplete finish. In other words, optical contact was insufficient to allow continuance of polishing until the complete removal of grayness.

---

‡ Refer to the footnote on page 122.

### 1.3.4. Stability of Optical Contact

The limit of protection by the first method using a pitch layer dissolved in lacquer thinner as shown in Figs. 5 (a), (b) is about 0.1 mm, while that of the second one using edge lapping and paraffin as shown in Fig. 5 (c) is about 0.06 mm. This is because the dissolved pitch layer or paraffin film come into contact with the pitch polisher during working, thereby causing minute damages to layers and their insufficient protection allows water to enter into the boundary surface of optical contact.

On the other hand, the third method of Fig. 5 (d) does not have the defect mentioned above and can protect the optical contact completely as stated before.

### 1.3.5. Deformation of the Finally Polished Surface in the Free State

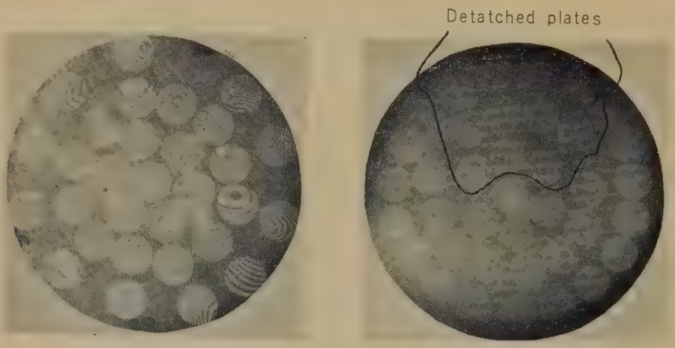
The finally polished surfaces were deformed convexly on these side as shown in Fig. 20. This phenomenon is quite contrary to the so-called Twyman effect,(9) that is, the deformation becomes concave on the polished side.

In the case of a thick plate, the height of at least 0.6mm is raised over the optical flat's surface, while in the polishing of plates of below 0.15 mm thick, the water-proof layer has a thickness comparable with that of the crystal plates. This originates scratchings by polishing abrasives embedded into the water-proof layers. Consequently, internal tensional strain caused by scratching—i.e.—internal compressive stress becomes larger on the finally polished surface side. As a result, tensional stress will be given to the same side for equilibrium, which will lead to the convex deformation on that side.

Concerning this point, discussions in detail will be made in Chapter 2.

### 1.3.6. Mechanical and Vibrational Properties of Quartz Plates Produced by Polishing

Flatness and parallelism of quartz plates were measured by "Multiple Beam Interferometry" ; examples being illustrated in Fig. 21. As seen from these fringes, plates whose finally polished surfaces have poor flatness are wedge-shaped, while plates having good flatness show unresolved Fizeau fringes : that is to say, the variation of thickness is of the order of 0.01 $\mu$ as shown in Fig. 22, which result was calculated from

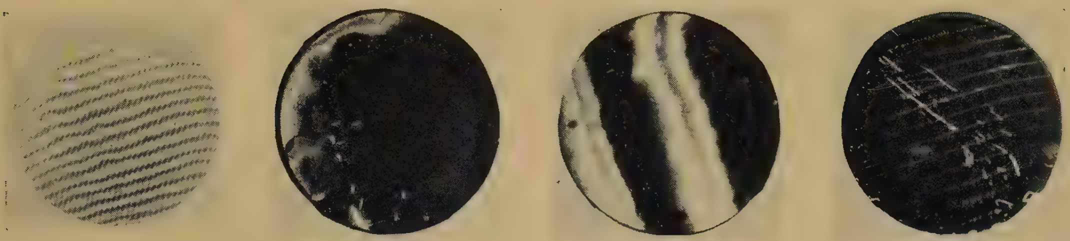


(a) $t$ 0.125 mm
in Experiment II

(b) $t$ 0.090 mm
in Experiment IV

Fringe Interval ≒ 0.3 $\mu$

**Fig. 20**—Convex deformation of finally polished surfaces in free state.

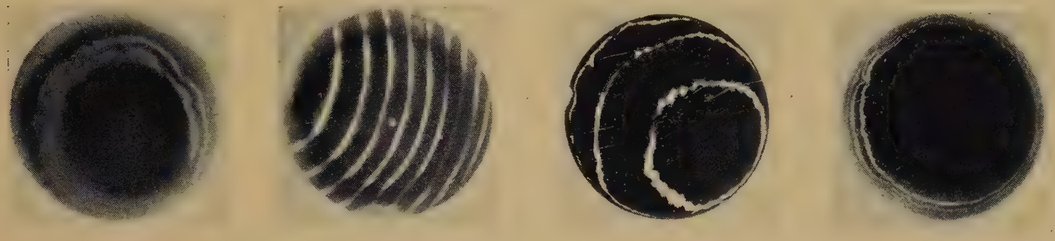


(a) $t$ 0.125 mm (Exp. I); Parallelism 3 $\mu$; 66 Mc (the 5 th) 80 Ω.

(b) $t$ 0.148 mm (Exp. III); Parallelism within 0.2 $\mu$, 79 Mc (the 7 th) 50 Ω

(c) $t$ 0.148 mm (Exp. III); Parallelism 0.2 $\mu$; 56 Mc (the 5 th) 37 Ω.

(d) the same as (b) Flatness 0.1 $\mu$.



(e) $t$ 0.092 mm (Exp. V), Parallelism 0 4 $\mu$. 90 Mc (the 5 th) 27 Ω.

(f) the same as (e), Flatness 0.5 $\mu$.

(g) $t$ 0.096 mm (Exp. VII); Parallelism witin 0.2 $\mu$; 120 Mc (the 7 th) 50 Ω.

(h) $t$ 0.035mm (Exp. IX); Parallelism within 0.1 $\mu$; 140 Mc (the 3 rd.) 14 Ω.

Fringe Interval ≑ 0.2 $\mu$ (in Parallelism), 0.3 $\mu$ (in Flatness)

**Fig. 21**—Multiple beam interference Fizeau fringes in transmission indicating mechanical quantities of quartz plates.

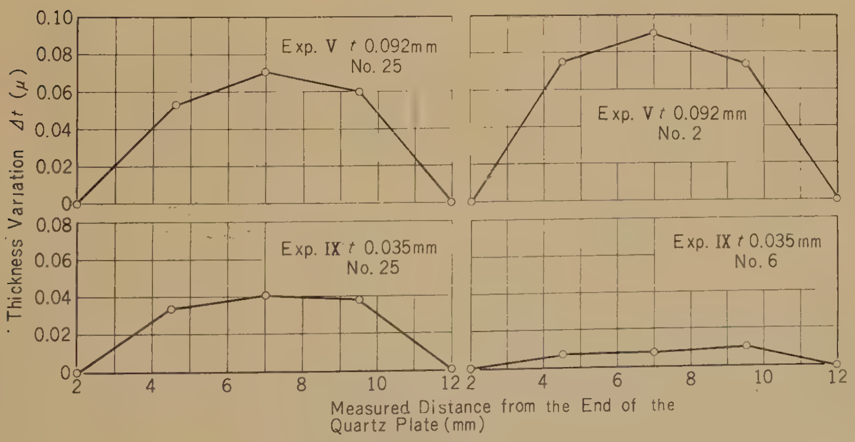


**Fig. 22**—Examples of thickness variations measured by Haidinger fringes.

Haidinger fringes.†

The effect of annealing may be clearly recognized from Fig. 21, and if this fact is taken into account with respect to the results shown in Fig. 20, it is seen that a kind of disturbance exists in polished layers even if the surface is finished to a high degree.

Distributions of flatness and parallelism measured on the greater part of the quartz plates are illustrated in Figs. 23 and 24.

Further, characteristics of the crystal units using these plates are shown in Fig. 25.(1)‡ From these results, it may be concluded that the polishing has given the desired results.

### 1.4. Summary

Development of a polishing technique for very thin oscillator-plates is described in this chapter. This may be summarized as follows:

(1) Problems in polishing were studied with the conclusion that the reciprocation should be the main motion in a lens polishing machine.

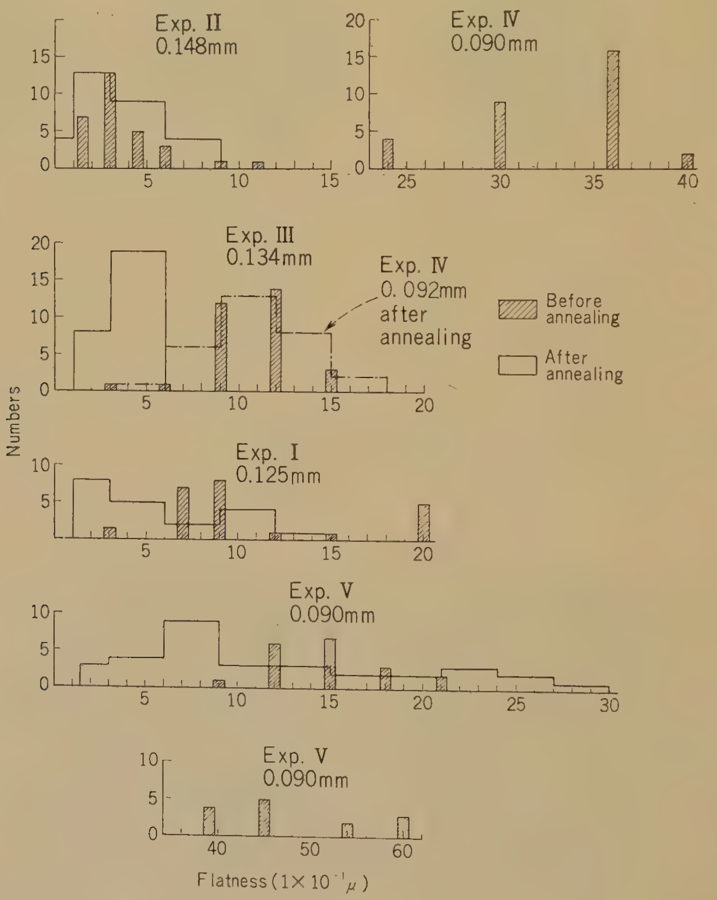


**Fig. 23**—Distribution of flatness of quartz plates before and after annealing.

---

† The variation of thickness can be expressed by the following equation: $\Delta t=t\{(D_1^2-D_2^2)/(8f^2n^2)\}$, where $t$ is plate thickness, $D_1$ and $D_2$ are the diameters of Haidinger fringes observed for the two positions of the plate whose thickness difference is to be measured, $f$ the focal length of the camera lens used, and $n$ the refractive index of the plate measured.

‡ Added subsequent data to ones which were illustrated in that reference (1) with values of IEC's specification.

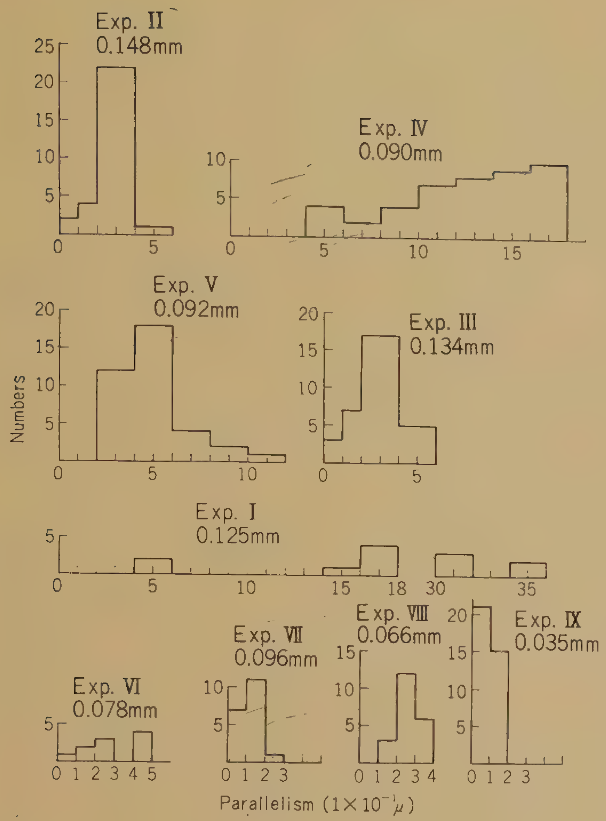


**Fig. 24**--Distribution of parallelism of quartz plates.

(2) A standard polishing process was established, and, especially for optical contact, the basis for polishing very thin plates of up to 0.035 mm thick was obtained by water-proof treatment ; who sefeature was the minute stepping by etching on the peripheries of plates.

(3) Conditions for adjusting parallelism‡ with maximum efficiency without giving rise to kink were laid down taking into consideration its dynamic relations to eccentric loading. In addition, convergence of parallelism was ensured to be within 1 μ through measurement by a pneumatic micrometer.

(4) That the accuracy varies with working conditions was made clear by the use of multiple beam fringes, and it was found that the measurement of thickness of plates in optical contact may be effected in a simple but precise way by means of an interferometer with stepped reference surfaces.

(5) From inquries into the results of experiments carried out from the view-point of working accuracy, parallelism and flatness of most plates proved to be of the order of 0.1 μ.

(6) As a result, it is now possible to obtain VHF crystal units for the frequency range of 60 to 140 Mc/s with sufficient activity and high yield, so that effect of polishing has thus been confirmed.

## 2. The Nature of Polished Quality Surfaces

In this chapter, paying attention to the deformation of thin quartz plates, the depth of the worked layer on the polished surface and the corresponding deformations of the plates are precisely explained. With the investigation of the stages of surface layers and of the analysis of residual stresses, estimation is made of the function of the secondary flaws.

Taking into consideration the polishing mechanism surmised from the above-mentioned results, the nature of polished quartz surfaces are discussed.

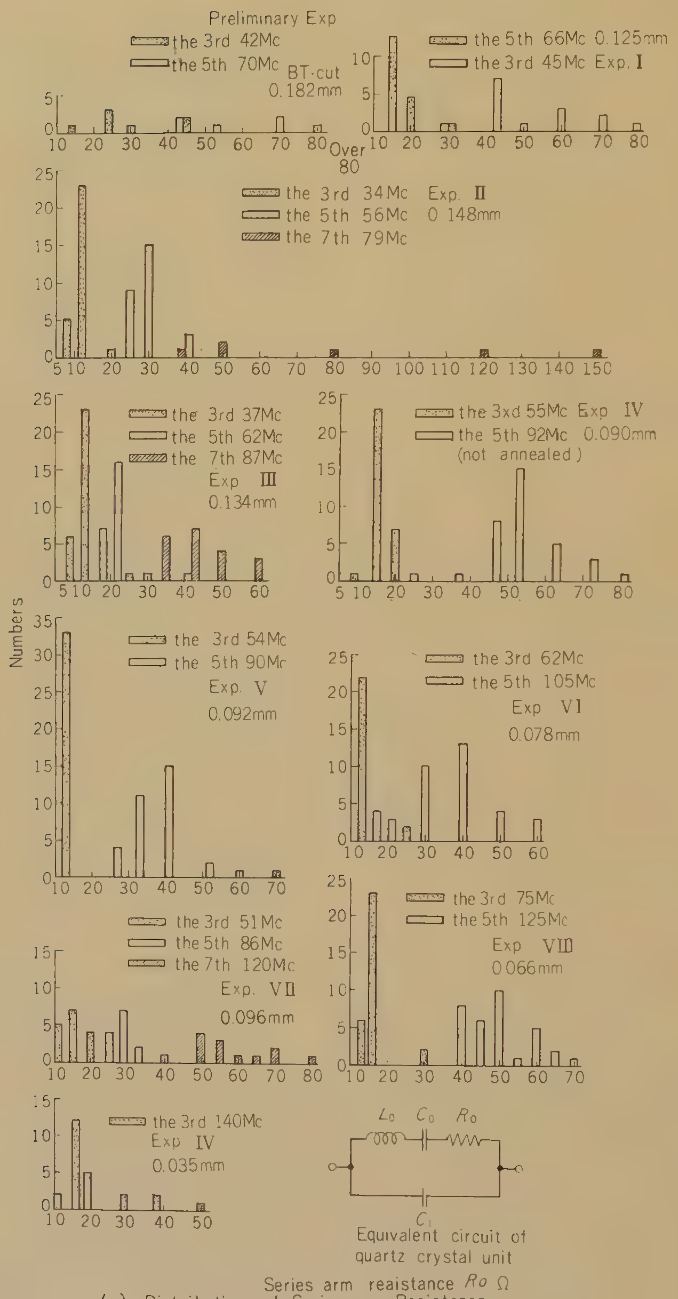
### 2.1. Experimental Apparatus and Method

### 2.1.1. Specimens and Their Working Conditions

AT and BT cut plates with dimensions of 14 mm dia. × 0.100 mm thickness, and X cut plates with dimensions of 15 mm(Y) × 14 mm(Z) × 0.0963 mm were obtained by the method and process described in Chapter 1. Also, AT and BT cut crystals of 14 mm in dia. and 4 mm in thickness, and X cut crystals of 15 mm × 14 mm × 2 mm thickness were used as specimens for measuring the depth of etching. These thick crystals were used to avoid deformation of the plates due to local etching.

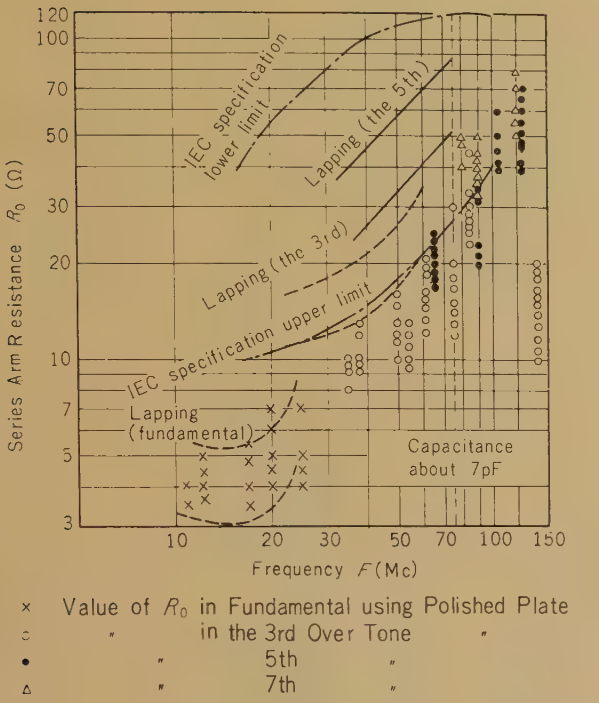
---

‡ Refer to the footnote on page 122.



(a) Distributions of Series arm Resistance
(by Takahara and Kobayashi)

Fig. 25 (a)—Characteristics of polished VHF crystal units.



(b) Comparison of polished crystal units with lapped crystal units in series arm resistance (by Takahara and Kobayashi)

**Fig. 25 (b)**—Characteristics of polished VHF crystal units,

### 2.1.2. Method of Etching

For tracing the deformation process of the plates at the time when one side of the polished surface is removed, the other side (of the polished surface) is covered with apieson compound, and then etched with a saturated solution of ammonium bifluoride in water which has been kept in a thermostatically controlled vessel. In this case, the etching temperature is kept at 27±0.2° C, while the etching time ranges from 1 to 400 minutes.

Washing is done with running water, distilled water and ethyl alchohol, while compound left on the surface is dissolved in lacquer thinner and benzine. When the etched depth is measured, the apieson compound covers the surface of the plate, whose past records are shown in Fig. 27, locally.

### 2.1.3. Measurement of Etched Depth

Since the "weight decrease" method only measures the average depth, the accuracy of this method is insufficient in the case of minute removal of surface layers in polishing, and moreover, its physical meaning is probably ambiguous.

Therfore, the interference method, whereby the depths can be obtained directly, is used mainly, and its application is made in the following ways:

(1) Fringes of equal chromatic order⁽⁸⁾ for etching times of 20 sec. to 1 min. for AT and BT cut crystals, and for etching time of below 50 minutes for X cut crystals.

(2) Multiple beam Fizeau fringes for etching time of 1–40 minutes for AT and BT cut crystals and for etching time of 50–200 minutes for X cut crystals.

In addition, the stylus method is applied to etching for the time ranging from 20 to 60 minutes for AT and BT cut crystals and from 200 to 400 minutes for X cut crystals. It is noteworthy that accuracies of the order of 10 Å can be obtained in measuring etched depth by this direct method.

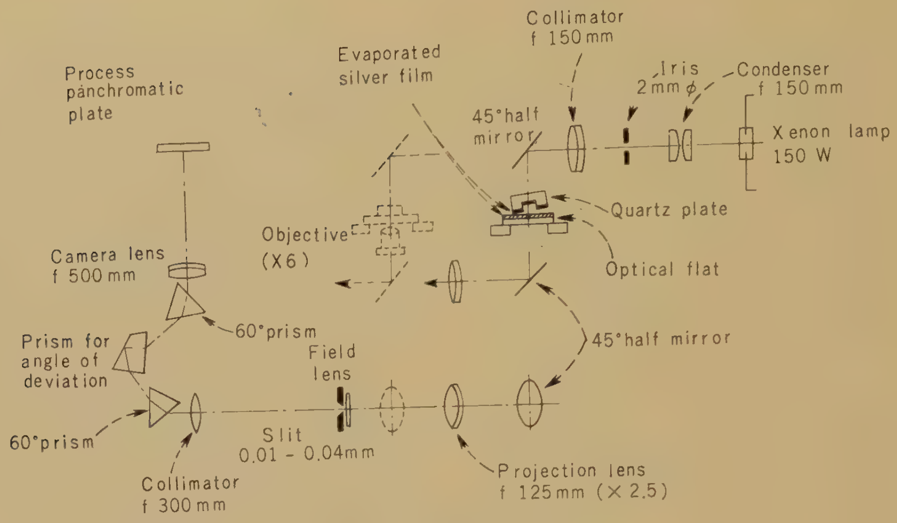
The interference apparatus using fringes of equal chromatic order and its optical arrangement is shown in Fig. 26, where two reflecting mirrors are used to obtain the white light Fizeau fringes in a horizontal position, with the three prisms also being used to make the fringe's dispersion larger.

The wave-length is determined by the Hartmann's dispersion formula as follows:

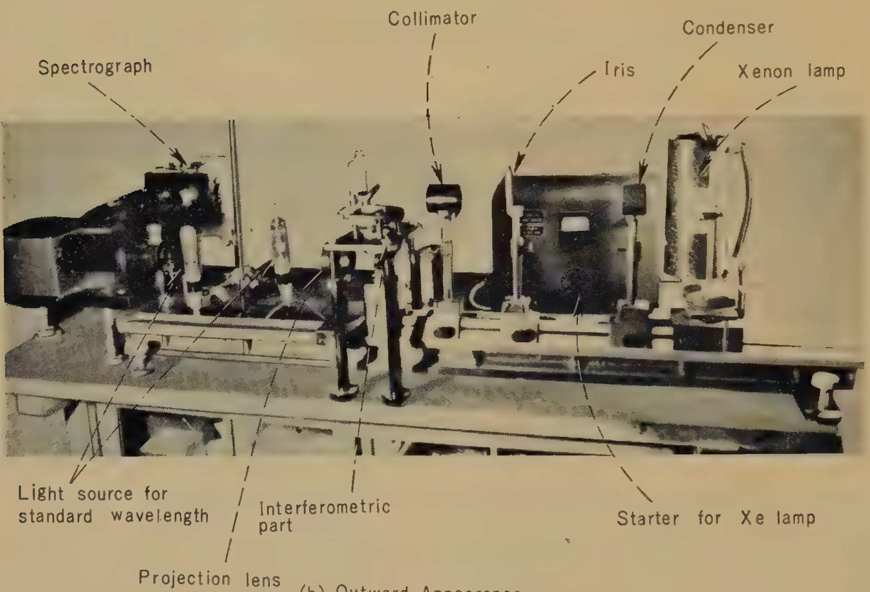
$$\lambda=\lambda_0+\frac{C}{d_0-d}, \qquad (1)$$

where $\lambda_0$, $C$ and $d_0$ are the constants of the spectrograph, which are to be determined by the standard wave-lengths (of Hg, Cd and Na in this case).

The etched depth $h$ is obtained from the following equation.



(a) Optical arrangement



(b) Outward Appearance

**Fig. 26**—The interference apparatus using fringes of equal chromatic order for measuring etched depth.

$$h=\frac{1}{2}\frac{\lambda' j+1}{\lambda' j-\lambda' j+1}(\lambda' j-\lambda j), \qquad (2)$$

where $\lambda' j$ and $\lambda j$ are the wave-lengths at etched and polished surfaces, respectively, with $\lambda'$ being longer than $\lambda$.

For Fizeau fringes, the apparatus shown in Fig. 8 of Chapter 1 is used.

### 2.1.4. Measurement of Deformation and Observation of the Crystal Surface

The same apparatus as mentioned above was used to produce the two-beam Fizeau fringes, as the lapse of time for evaporation or other treatments should be avoided so that no change may be caused to circumferential conditions.

In determining the flatness of a plate, after making an oblique projection as a function of $\lambda/2$ through a certain section of a plate, a deflection curve is converted to the direction which connects both the intersecting points of the sectional line with edges of a plate. Thus, the maximum deflection in this curve forms the flatness* as shown in Fig. 27.

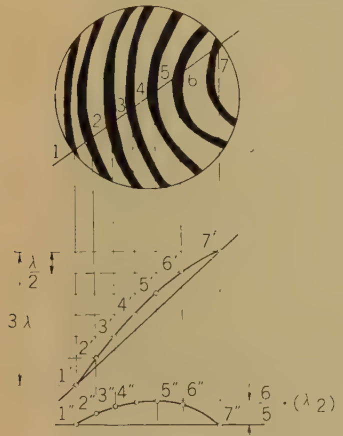


**Fig. 27**—Determination of flatness from interference fringes.

In connection with deformation of plates, states of surfaces are observed, with the same positions to be traced by a phase contrast microscope in transmission and by a dark field reflection microscope with a magnification of 100 to 400. Moreover, a few plates were inspected with an electron microscope.

### 2.2. Deformation Process of Worked Surfaces by Etching

#### 2.2.1. Relation between Etching Time and Etched Depth

Some examples of etched states measured with the interference fringes are shown in Figs. 28 and 29. From these results it is made clear that very sharp steps are obtained in AT cut crystals, while ambiguous boundaries are shown in X cut crystals.

In fringes of equal chromatic order, it is found that Equation (2) holds good between wave-length and thickness, while the etched depth is, as shown in Fig. 30, expressed as one half of the difference between the coordinates of two parallel lines having the notation of $N\lambda$ and $N\lambda'$, respectively ; in which case the $\tau(\lambda)$ function of Köester⁽⁹⁾ is applied.

Total results of these relations are shown in Fig. 31, which may be summarized as follows:

$$h_{AT}=200t^{0\cdot74}\quad\text{for 20 seconds to 40 minutes}\qquad(3)$$

$$h_{BT}=135t^{0\cdot50}\quad\text{for 20 seconds to 30 minutes}\qquad(4)$$

$$h_{X}=18t^{0\cdot55}\quad\text{up to 50 minutes,}\qquad(5)$$

where $h$(Å) is the etched depth and $t$ (minute) is the etching time.

The above relation of the power function corresponds qualitatively to that of the depth of the boundbary zone of blue "stain" on untreated glass surfaces found by Kinoshita and Natsume.⁽¹¹⁾

A relatively large etched depth in an early stage of the etching suggests in a way a change in the nature of the surface layer. Moreover, an increase in inclination in the latter half of the curves for AT and X cut crystals is considered to be caused by the removal of secondary flaws and etched patterns which will be described later.

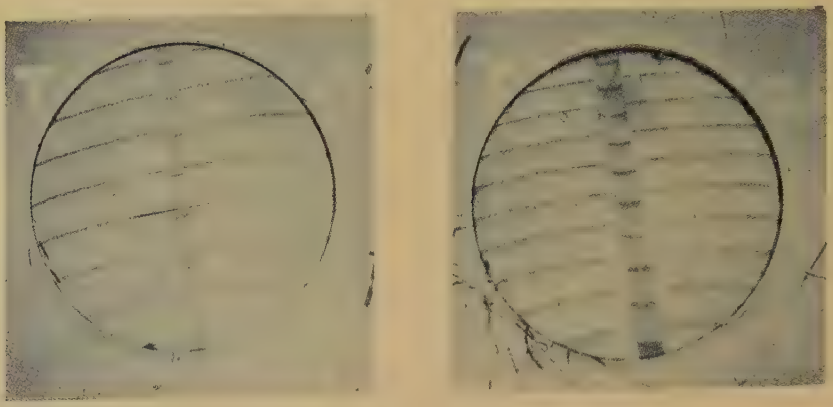
Furthermore, very small etched depths in X cut crystals may be due to the close arrangement of atoms in the direction of thickness, which makes the resistance against chemical action stronger.

#### 2.2.2. Deformation Process of Lapped Surfaces by Etching

In order to find the thickness of specimens

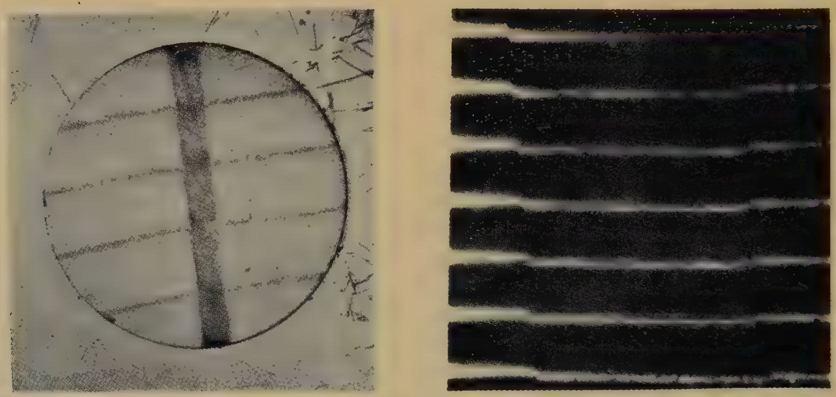
---

* Taken as + for convex and as − for concave surfaces.



(a) Etching Time 4 min (in Reflection).

(b) Etching Time 12 min (in Reflection).



(c) Etching Time 30 min (in Reflection).

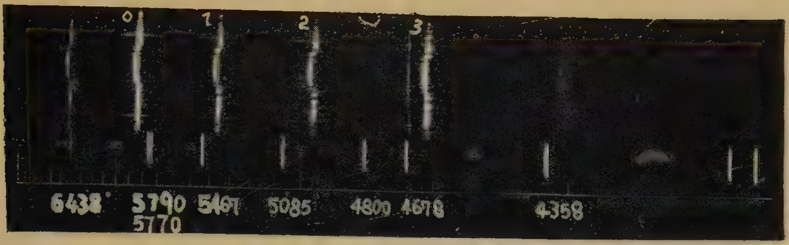
(d) Etching Time 2 min (in Transmission); × 30.

Fringe Interval ≒ 0.3 μ

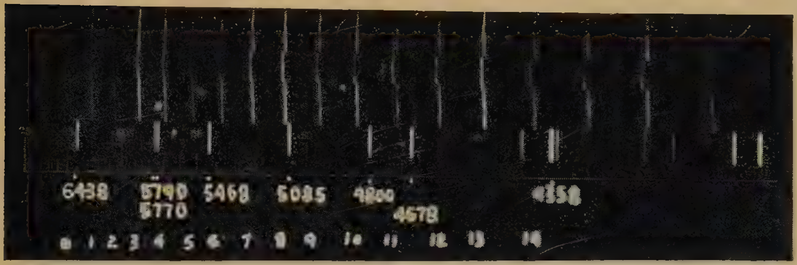
**Fig. 28**—Examples of etched depths by multiple beam Fizeau fringes in AT-cut crystals.

suitable for the measurement of deformation, the deformation process was first investigated on a lapped surface obtained by lapping with Green Carborundum No. 600.

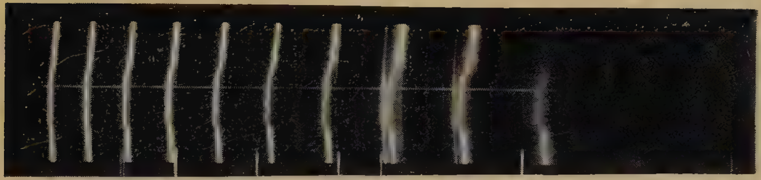
Fig. 32 shows the results of measurements by the "weight decrease" method, from which the lapped surface is found to be unstable in comparison with the polished surface. On the other hand, the average etched depth is small compared with the roughness of 7 to 8 μ of a lapped surface; that is to say, etching seems to be done only on the raised part of surface, even at the average depth of 1400 Å, when deformation is essentially completed as shown in Fig. 33 (a). In general, it is expected that the rough surface will have a large etched depth because of the increase of surface area, but it is necessary for satisfying this to assume an equal etching rate for each depressed and raised part. Despite the high etching rate in residual cracks on the lapped surface, the average depth was obtained from



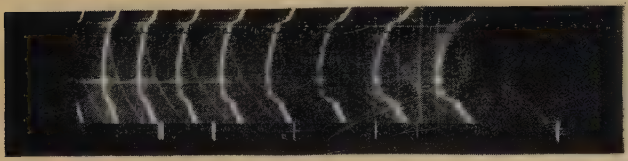
(a) Etching Time 20 sec AT-cut



(b) Etching Time 1 min AT-cut



(c) Etching Time 3 min X-cut



(d) Etching Time 10 min X-cut

**Fig. 29**—Examples of etched depths by fringes of equal chromatic order in transmission.

the total weight decrease and the apparent plate area, and was too small.

Since the lapping causes an aggregation of tensional fractures in such a brittle material as quartz, residual tensional strains are left over near cracks, and, as a result, residual stresses become compressive on account of the restriction of material itself. For equilibrium of these residual stresses, additive stresses occur through bending of the plate, which give lapped surface tensional stresses and the other surface (unworked) compressive stresses. As a result, if the surface already polished is lapped, it will be deformed convexly on the lapped side (concavely on the polished side) as shown in

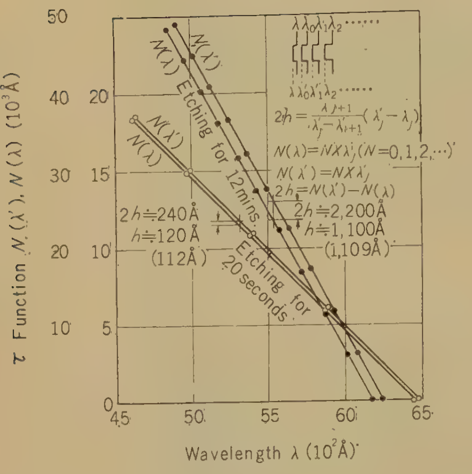


**Fig. 30**—Calculation and check of etched depths by the τ function.

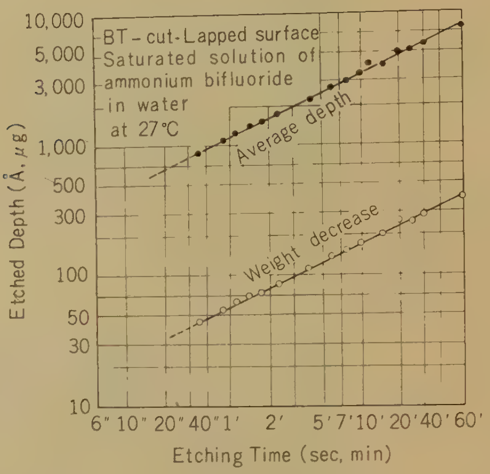


**Fig. 32**—Curves of etched depths (lapped surface).

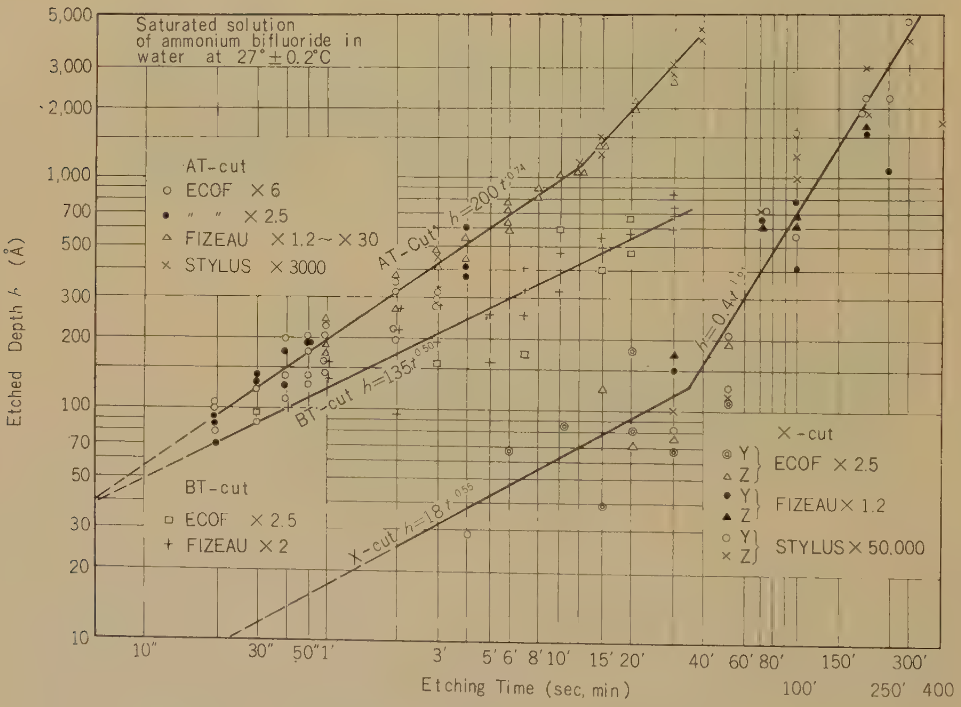


**Fig. 31**—Curves of etched depths.

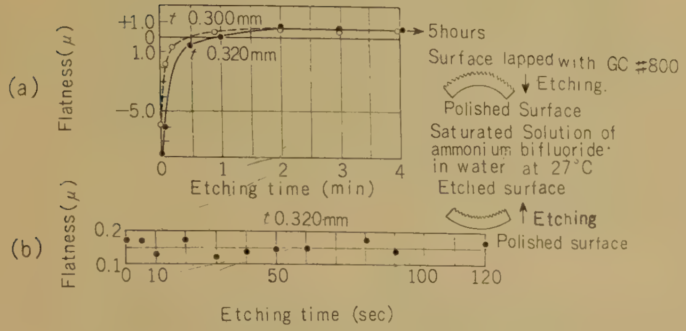


**Fig. 33**—Deformation process of lapped surface by etching.

Figs. 34 (a) and (b). Etching applied in this stage will cause lapping stresses to be removed ; which will, as seen from Fig. 34 (c), lead to the decrease of concavity on the polished side because of the decrease of additive tensional stresses.

After passage of reversed curvature, compressive stresses are added on the polished side on account of larger stresses or that side; that is to say, the lapped surface becomes concave, as seen in Fig, 34 (d).

The continued etching will cause the completion of deformation at this thickness, by removing for the most part of these residual lapping stresses ; and this theory is supported by the appearance and increase of etched patterns shown in Figs. 34 (e) and (f), respectively.

Now, in the case of etching of a polished surface, the bending force and bending moment produced by polishing stresses is not so large that a plate will not be deformed at that thickness as shown in Fig. 33 (b). It is, therefore, clear that thinner plates should be used for tracing the deformation process of a polished surface.

From the results mentioned above, it may be explained that the Twyman effect depends on the origination and removal of the residual lapping stresses which are compressive.

### 2.2.3. Deformation Process of Polished Surface by Etching

Fig. 35 shows the examples of variation in curvature of an un-annealed AT cut crystal, while Fig. 36 illustrates the deformation process of AT and BT cut crystal which are not annealed. It may be noticed from these results that the reversion of curvature occurs nearer to the surface as compared to that of a lapped surface, and then, the gradually changing stage is long after reversion.

In Fig. 36, etching on convex surfaces ($E_{p1}$) leads to obtaining reversed times ranging from 1.5 to 4 seconds, which correspond to etched depths of 20 to 30 Å from Equation (3).

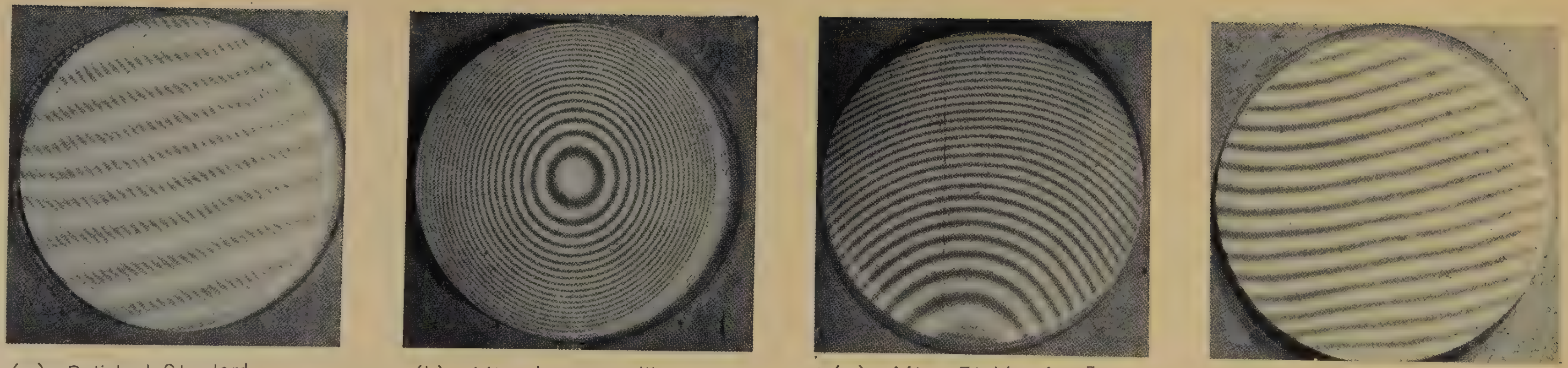
On the other hand, since the gradually changing stage does not exceed several minutes, the corresponding depth is of the order of several hundreds of Angstroms.

Now, when the former standard surface (optically contacted) is etched, its deformation will follow the $E_{p2}$ curve indicated by the dotted line in Fig. 36. Since the improvement of flatness is the same as that of $E_{p1}$ in spite of its slight degree of change, stresses of the same kind are also left over on this side.

Slopes of the deformation curves of annealed plates will be opposite as shown in Fig. 37 according to whether the concave or convex surface is etched first, while the degree of deformation is about one-third of that in un-annealed plates, with no reversion of curvature to be seen.

It is, therefore, suggested that stresses are released through annealing, and the deformation is caused by mechanical disturbance.

In X cut crystal plates, anomalous deformation processes could be seen as shown in



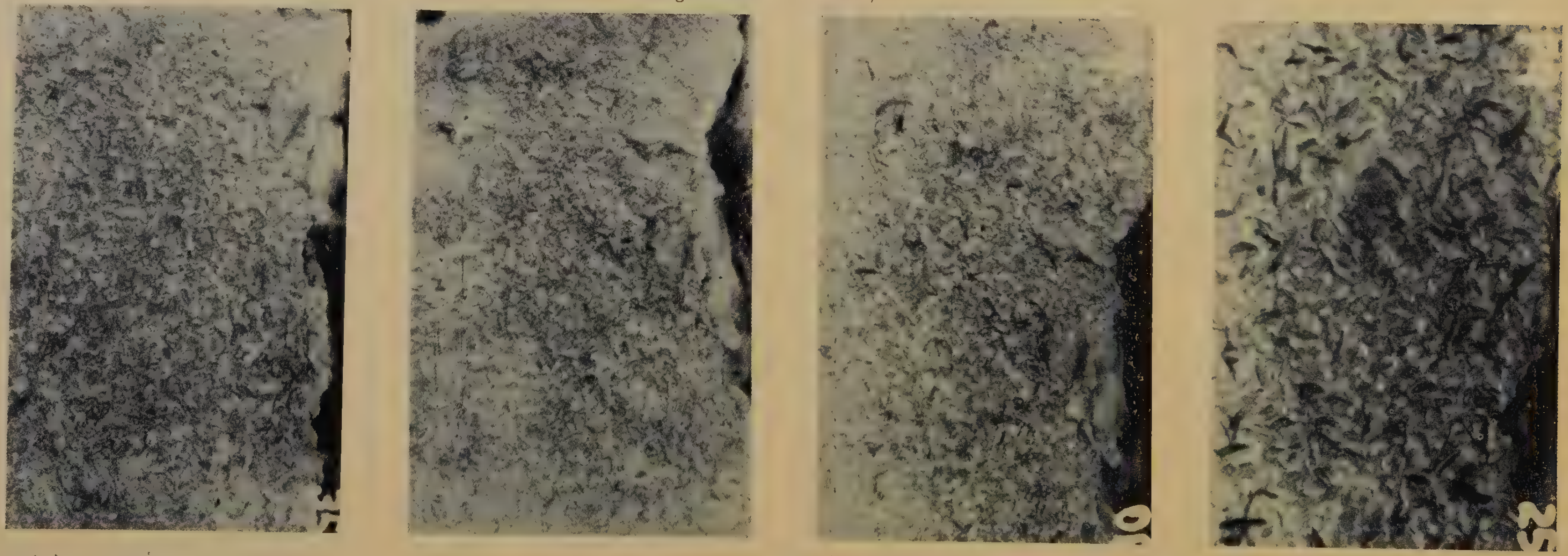
(a) Polished Standard Surface before Lapping. $+0.1\,\mu$

(b) After Lapping with GC # 800. $-6\,\mu$

(c) After Etching for 5 Seconds. $-2\,\mu$

(d) After Etching for 50 seconds. $+0.2\,\mu$

Fringe Interval $\fallingdotseq 0.3\,\mu$



(e) Lapped Surface after Etching for 10 Seconds.

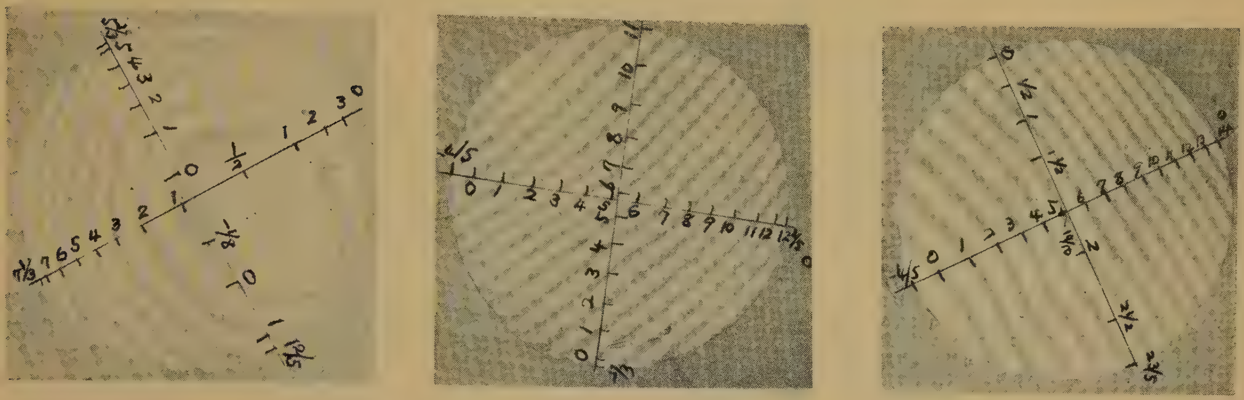
(f) Lapped Surface after Etching for 1 Minute.

$10\,\mu$

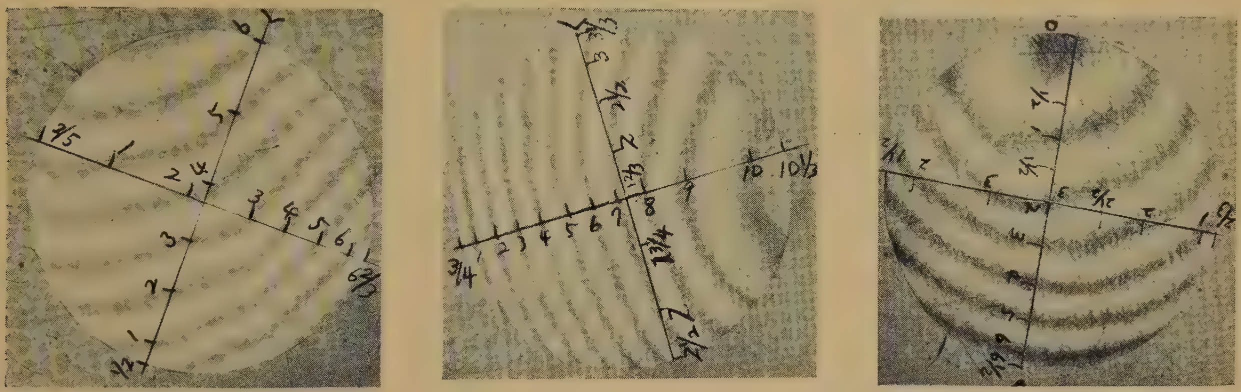
(g) Lapped Surface after Etching for 5 Minutes.

(h) Lapped Surface after Etching for 1 Hour.

**Fig. 34**—Release of deformation and change of surface states in lapped surfaces by etching.



(a) Etching 0 sec (b) Etching 2 sec (c) Etching 20 sec



(d) Etching 2 min (e) Etching 7 min (f) Etching 20 min

Fringe Interval ≒ 0,3 μ

**Fig. 35**—Release of deformation of polished surfaces by etching. AT-cut crystals, 0.100 mm.

Fig. 38, when the standard surface was still a polished one. This is because of the release of skin stresses on the protected side, which originates from etching. Moreover, the interpretation of this phenomenon is supported by the results shown in Fig. 42 that the descending tendency of deformation appeared after etching for 2 to 4 minutes in the case of a polished standard surfaces, but such an anomaly did not appear in the case of etched standard surfaces. Thus, the specimens whose standard surfaces had been etched were used for analyzing residual stresses.

Deformation processes of X cut crystal plates are, in general, similar to those of AT and BT cut crystal plates as shown in Figs. 39 and 40, while the changes in the intermittent stages are not violent because of the localization of stresses at the skin.

Now, when the process is modified into the relation between the difference of flatness whose standard is fixed at the initial flatness (called the degree of deformation) and the etching time, the results will be as indicated in Figs. 41 and 42. Evidently, the deformation process has three stages, in which kinks are considered to mean the kind of influence and its changes existing in surface layers, while their inclinations are

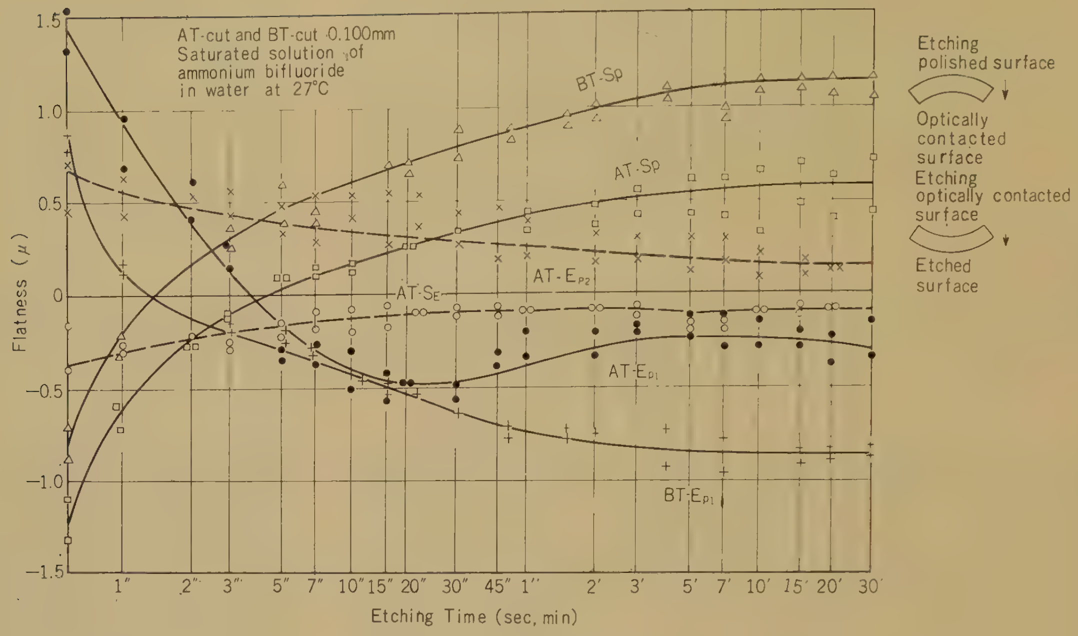


**Fig. 36**—Deformation process of polished surfaces by etching (not annealed).

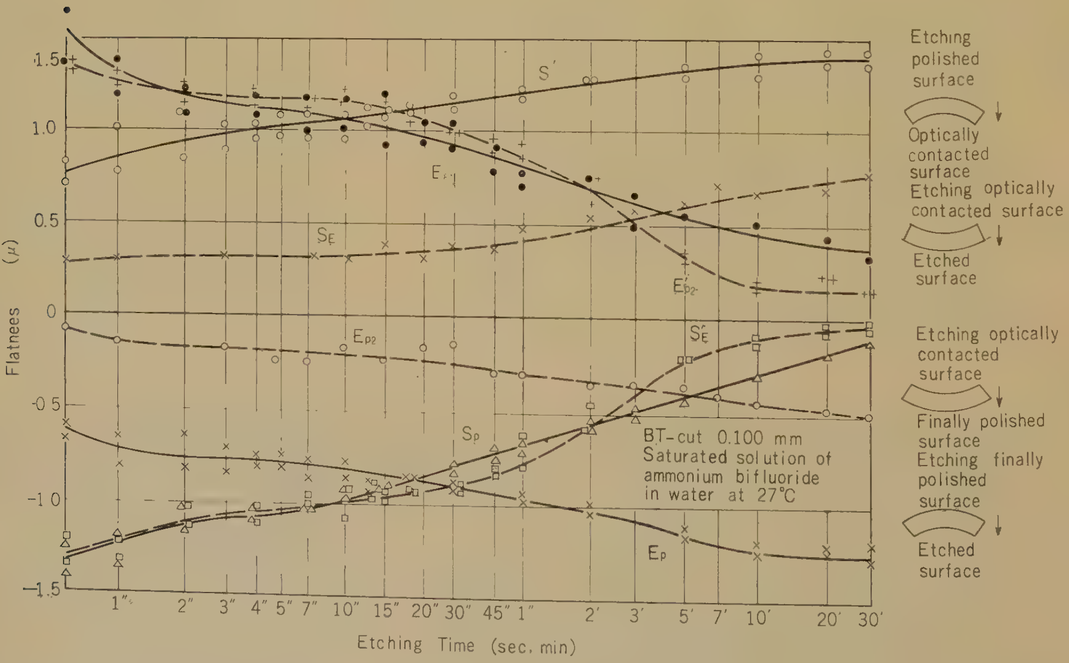


**Fig. 37**—Deformation process of polished surfaces by etching (annealed).

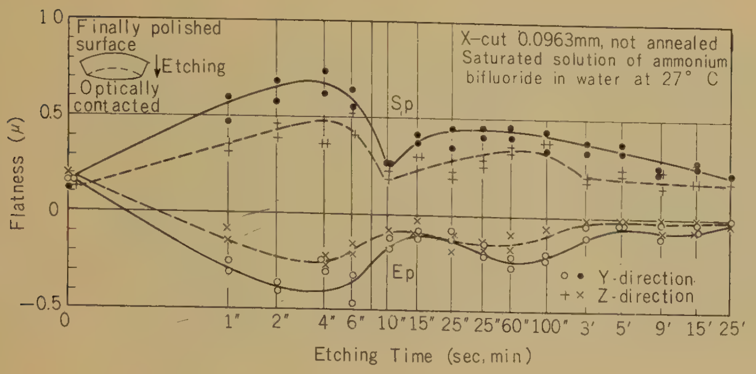


**Fig. 38**—Anomalous deformation process of X-cut crystal plate by etching.

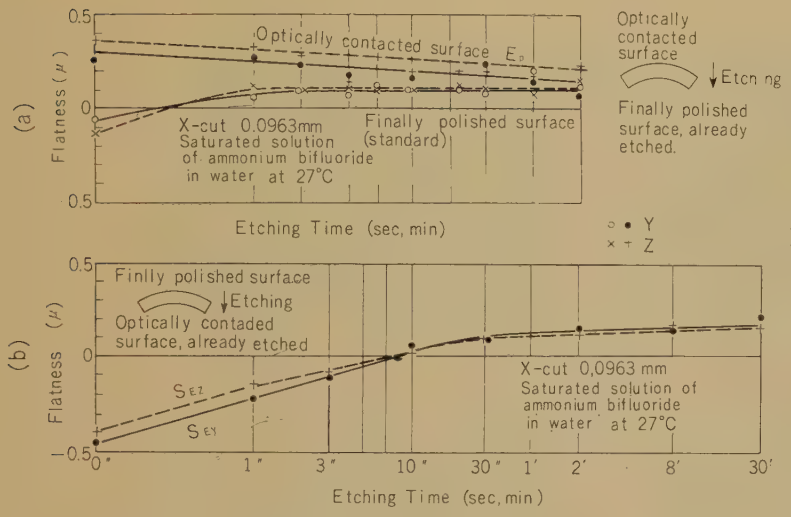


**Fig. 39**—Deformation process of polished surfaces of X-cut crystals by etching (not-annealed).

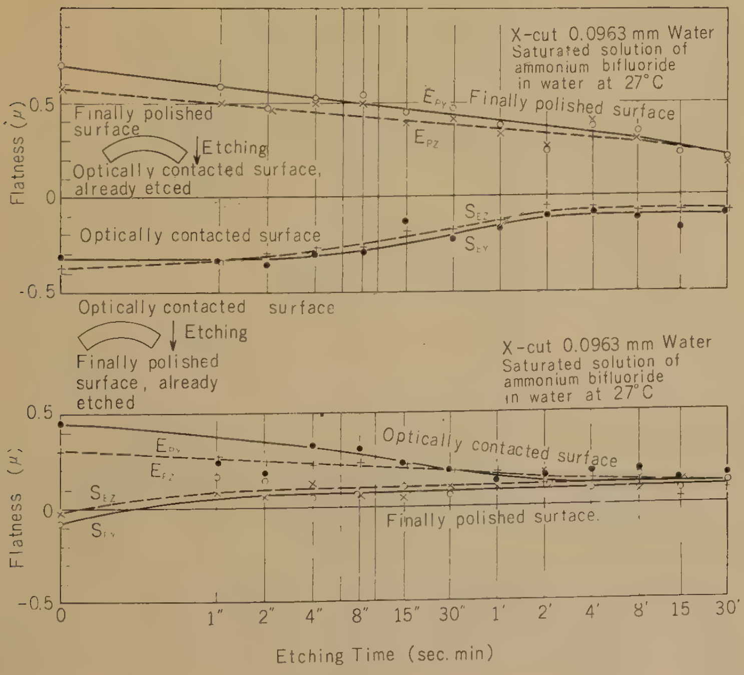


**Fig. 40**—Deformation process of polished surfaces of X-cut crystals by etching (annealed).

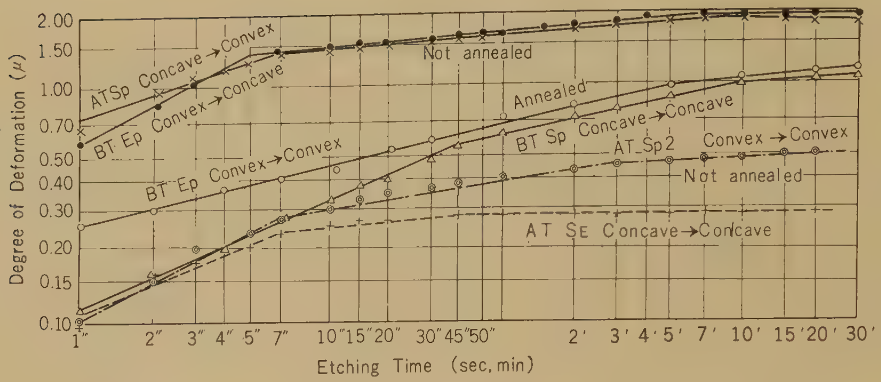


**Fig. 41**—Curves of degree of deformation, thickness 0.100 mm (AT-cut and BT-cut crystals).

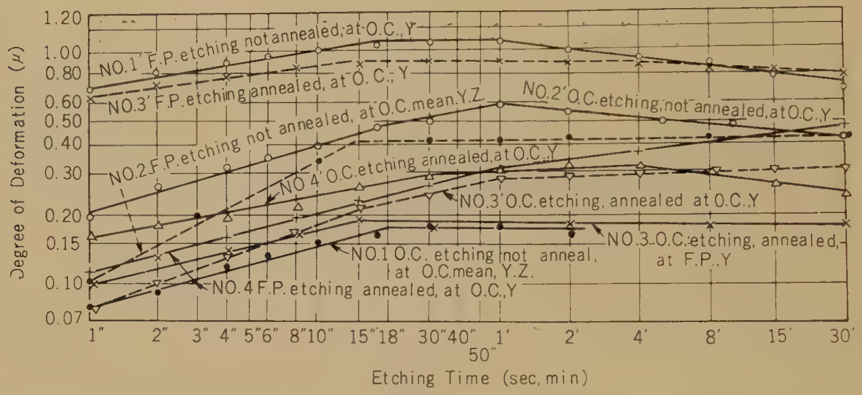


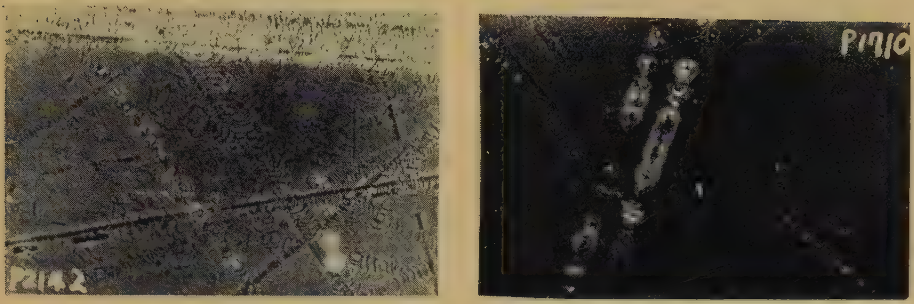
**Fig. 42**—Curves of degree of deformation, thickness 0.0963 mm (X-cut crystals).

explained to be determined only by the thickness of plate.

The effect of annealing makes stresses in the first stage approach stresses in the gradually changing stage, while the corresponding depths in this stage vary with the orientation, and the depths in AT cut crystals are greater than those in BT cut crystals. Moreover, in the case of X cut crystals, the first kink is distributed over the time ranging from 15 seconds to 1 minute, where the depth corresponding to the gradually changing stage is small as shown in Fig. 42. That is to say, the second stage is indistinguishable from the first one because of the localization of stresses at the skin.

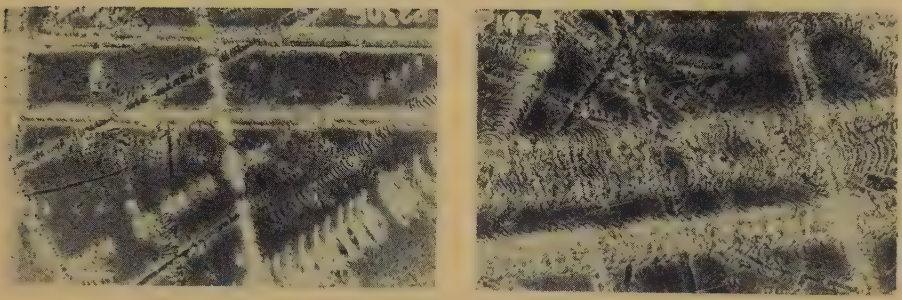
Also, from observations, secondary flaws appearing perpendicularly to the scratching direction are noticed as shown in Figs. 43 and 44. They are perceived about 45 seconds after the start of the etching process, become rather clear after about 3 to 5 minutes, and then make their complete appearance after 10 to 20 minutes when viewed through a phase contrast microscope with a magnification of 400.

From these appearances and deformation processes, it may be considered that the secondary flaws produced on surface layer have an influence on the deformation in the gradually changing stage. On the other hand, when the finally polished and optically contacted surfaces are both etched for the same etching time, many secondary flaws



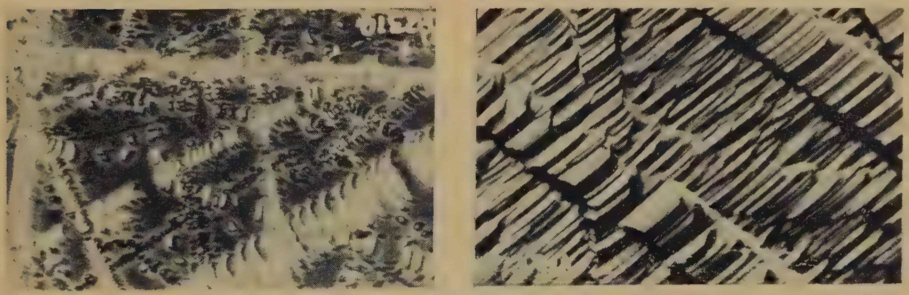
(a) After Etching for 3 Minutes.

(d) At Optically Contacted Surface after Etching for 5 Minutes.



(b) After Etching for 7 Minutes.

(e) At Finally Polished Surface after Etching for 5 Minutes.



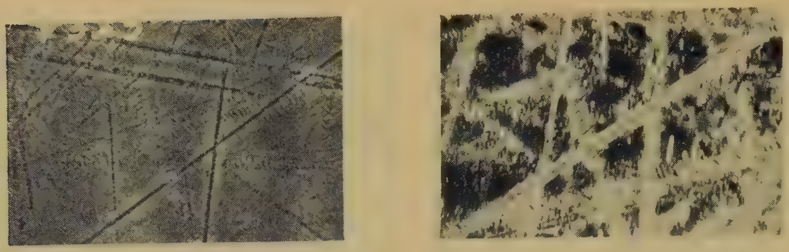
(c) After Etching for 30 Minutes.

(f) Previous Record of Scratching after Etching for 5 Hours.

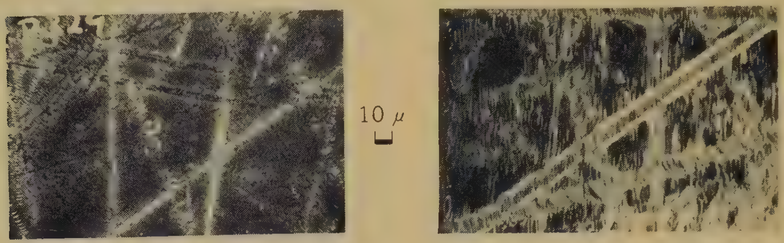
**Fig. 43**—Secondary flaws in polished AT-cut crystals.

will be found occuring on the surface of the former. Moreover, by deep etching for 1 to 5 hours, the past records of scratching can be observed as tracks, even in case the etched patterns of the crystal have already appeared.

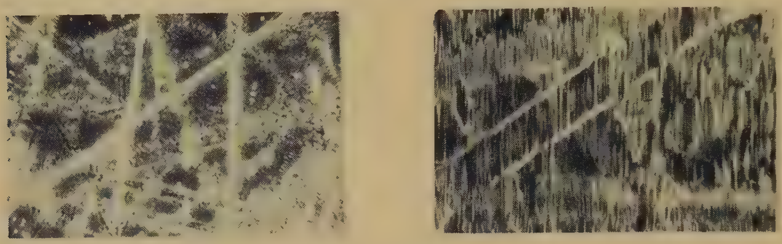
Although such parts may grow in depth by etching, their initial depths before etching are estimated to be 200 to 10,000 Å for AT cut crystals and about 120 Å for X cut crystals, as will be discussed in detail later. Besides, as seen from the secondary flaws in Fig. 44 (g), their pitches and angles to the scratching direction are almost constant as to one scratching line, whose cause is considered in the scale model test for secondary flaws caused by scratching in Section 2.3.



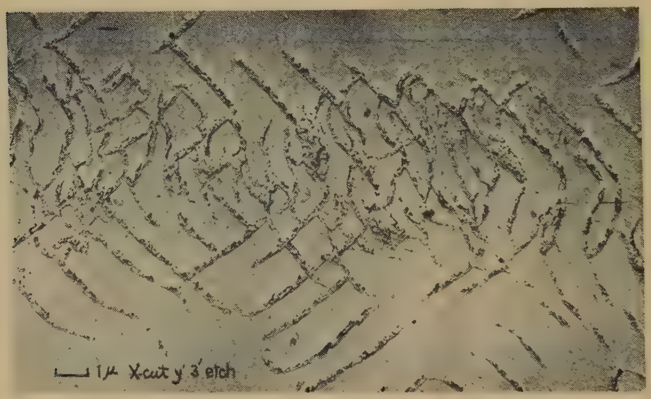
(a) After Etching for 2 Minutes. (d) Afer Etching for 70 Minutes.



(b) After Etching for 10 Minutes. (e) After Etching for 180 Minutes.



(c) After Etching for 25 Minutes. (f) After Etching for 400 Minutes.



(g) After Etching for 3 Minutes. Electron Microphotograph.

**Fig. 44**—Secondary flaws in polished X-cut crystals.

### 2.2.4. Mutual Relation between the Deformation Processes and the Nature of Residual Stress

By arranging the results shown in Figs. 36, 37, 39, and 40, it may be seen that the flatness improves with etching for convex surfaces, while it becomes worse with etching for concave surfaces. The mutual relations among these curves may be explained by the existence of residual compressive stress in the skin layer. That is, the reason why plates become convex is that added tensional stress is necessary for

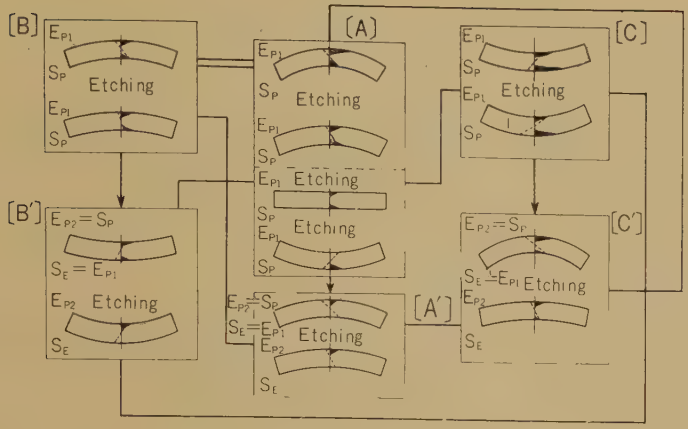


**Fig. 45**—Relation of curvature variations to deformation processes.

equilibrium on the side of the plate where the larger residual compressive stresses are left. These conditions are illustrated in the upper left, upper middle and lower right diagrams of Fig. 45. Now, the deformation processes by etching are explained as follows :

[A] Residual stresses on polished layers decrease with etching and, as a result, tensional added stresses also decrease to make the convex surface become similar to the flat one. During this process, a plate can be flat when the stresses on both sides become equal. With the etching continued, residual compressive stresses become relatively large on the standard surface, which will lead to the increase of added tensional stresses on that side. As a result, the etched surface must deform concavely. Thereafter, the concave surface will increase its degree of concavity until the deformation is completed due to the removal of stresses by etching, with the plate being of the same thickness. Furthermore,

[A′] etching of the opposite side will improve the flatness just in the same way as in the case of [A] through removal of compressive stresses, although initial stresses are smaller than those of [A]. In this case, since the standard surface has already been etched, the accelerating effect caused by stresses on this sidemay be negligible, which will lead to the gentle-sloping inclination of deformation curves.

[B] Through the etching of the convex surface of the annealed plates, the curvature does not reverse because of the decrease in stresses even with plates of the same thickness as in the case [A]. After all, the deformation of a plate will be saturated, with its state of convexity remaining unchanged, its process being to be the same as in the first half of [A].

[B′] When the opposite side is etched, compressive stresses on that side will be decreased so that such stresses will be given to the etched surface in order to keep balance with the initial residual compressive stresses on the standard surfaces. This process is similar to that described in the latter-half of [A], with the exception of the acceleration of deformation by the opposite surface.

[C] In the case of the etching of concave surfaces in annealed plates, the tendency is the same as that of [B′], except the existence of the effect of acceleration on the standard surface.

[C′] Etching of the opposite side leads to the tendency which is also similar to that of [B], [A′], and that described in the first-half of [A], except the non-existence of the effect of acceleration.

It has been made clear from these results, that the decrease of convexity (equal to the increase of concavity) exists in the relation between the curvature and deformation process of plates in etching, and that compressive stresses must be left over on the polished surface.

### 2.3. Scale Model Test for Secondary Flaws Caused by Scratching

It was found that secondary flaws existed in polished layers of quartz, which were considered to play main part in the gradually changing stage of deformation.

Therefore, by making the scale model test of secondary flaws caused by scratching, deformation process of scratched surfaces were compared with that of polished ones, with inquiries into the origination mechanism of such secondary flaws made at the same time.

### 2.3.1. Specimens and Experimental Method

Specimens of AT cut crystal with the dimensions of 15 mm × 15 mm × 0.155 mm were polished under the conditions described in Chapter 1. Their surfaces were scratched with such points as diamond and sapphire styli or single Alundum abrasive with loads of 3 to 100g and scratching speeds of 0.3 to 1.5 mm/sec, making use of a surface roughness meter.

### 2.3.2. Origination of Secondary Flaws by Scratching

The results of the experiment performed to make secondary flaws by scratching are shown in Tables 3 and 4, in which an attempt was made to find out various conditions for producing the flaws that are similar to the ones to be produced by polishing.

With a sapphire-tipped stylus secondary flaws which are almost perpendicular to the sliding direction appeard before etching under load of over 30g, and they were exposed clearly to the view through etching (Fig. 46 (a)).

On the other hand, when a diamond-tipped stylus was used, secondary flaws having a close pitch came out under the load of 50g and they were accompanied with concoidal fractures (Fig. 46 (b)). Moreover, when the single Alundum abrasive was used, the shapes of the scratches had a resemblance to the ones which are produced in polishing as shown in Fig. 46 (c), while, on the fractured surface of the crystal (Fig. 46 (d)) or on the mechanically rubbed *r*-surface (Fig. 46 (e)), secondary flaws were also originated. These facts lead to the confirmation that secondary flaws are directly

**Table 3**

ORIGINATION OF SECONDARY FLAWS BY SCRATCHING (I)

Scratching Speed 1.5 mm/sec, Etching Time 7 Minutes

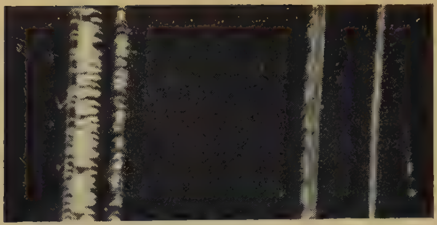
| Scratching Point | Load (g) | Number of Scratching Lines | Surface Stale |
|---|---|---|---|
| Diamond | 20 | 3 | Scratched traces seen before etching |
| | 10 | 2 | Detected Scratched traces seen after etching |
| Sapphire | 20 | 3 | Scratches did not appear |
| | 10 | 2 | Scratches did not appear |
| | 30 | 3 | Secondary flaws seen before etching, and exposed to the view by etching |
| | 50 | 3 | |
| | 100 | 3 | |

**Table 4**

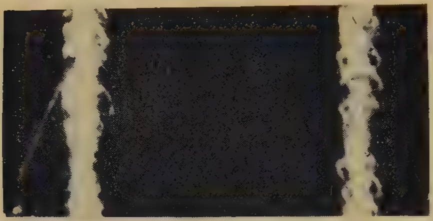
ORIGINATION OF SECONDARY FLAWS BY SCRATCHING (II)

Etching Time 7 Minutes

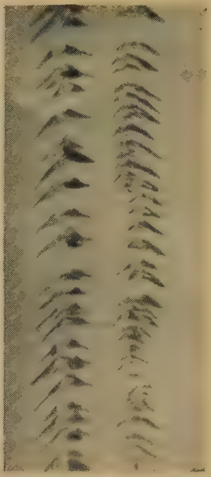
| Scratching Point | Specimen | Scratching Speed mm/sec. | Load (g) and Number | Surface State |
|---|---|---|---|---|
| Sapphire | No. 1 | 0. 3 | 50- 3 | Relatively continuous scratches and secondary flaws were found. The second scratching line revealed obscure traces and the third one did not appear, A scratching point was divided into three or four points. |
| | | | 30- 3 | The first line made secondary flaws whose pitch was small. But the second and the subsequent lines originated the scratched traces with secondary flaws intermittently. |
| | | | 20- 3 | All scratches showed lines without secondary flaws. |
| | | | 10- 3 | The existence of scratch was not clear. |
| | No. 2 | 0. 6 | 50- 5 | Before etching, scratches traces were found, and after etching secondary flaws were also seen. The second line showed secondary flaws, too, but their length was small. |
| | | | 30- 5 | No trace by etching. |
| | No. 3 | 0. 3 | 50-10 | Lines were scratched with a more normal contact angle than the one mentioned above. The point split into four points, thereby making scratched traces. |
| Diamond | No. 4 | 0. 6 | 50- 3 | Continuity of scratched traces with concoidal fractures was found, whose parts consisted of secondary flaws with a more roundish shape than those caused by the sapphire point. |
| | | | 30- 3 | The condition was almost similar to that mentioned above. However, secondary flaws were originated intermittently in one direction. |
| | | | 20- 3 | Scratches seemed to be just scale lines, whose width was about one-thirds of that of the lines obtained at 50g-3 lines. |
| | | | 10- 3 | The state was almost similar to that in the case of load of 20g, but the width obtained was nearly two-thirds of the latter. Secondary flaws were not recognized. |



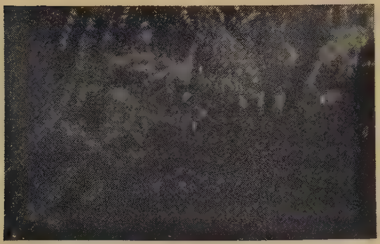
(a) By Sapphire Point, 50 g, × 270.



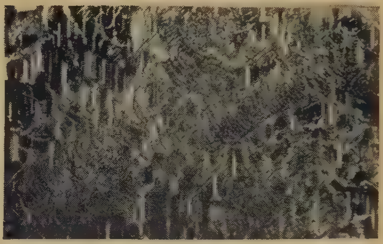
(b) By Diamond Point, 50 g, × 270.



(c) By Single-Grain Alundum, 50 g, × 270.



(d) Mechanically Damaged Surface, Etched for 15 Minutes, (Celluloid Replica), × 200.



(e) Natural r Surface (Celluloid Replica), × 200.

**Fig. 46**—Secondary flaws by scratching and mechanical damage.

related to the fracture.

### 2.3.3. Mechanism of the Origination of Secondary Flaws

In the state of scratching, contact circles are produced around the scratching point as shown in Fig. 47, and compressive stresses originate in the circular direction and within the circle, while tensional stresses originate in the radial direction, as Hertz originally indicated.(12)

Therefore, behind the proceeding point, tensional strains or fractures are left over due to the low tensile strength of quartz to tensional stresses. In these parts, secondary flaws, whose resistance against chemical

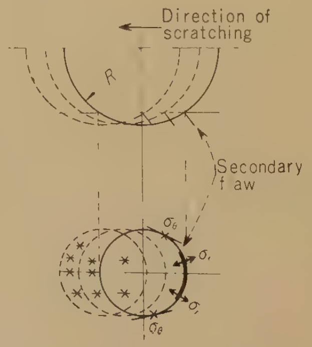


**Fig. 47**—Origination of secondary flaws.

action is small, will appear after etching.

From the observation of pitches of secondary flaws, it may be found that they are considerably constant. It is of course, first of all due to the accumulation and release of fracture energy, while the rough or fine interval of a flaw's pitch is related to the fracture of the scratching point. That is to say, unless the tensile strength of quartz exceeds the fracture limit during scratching, smooth tracks will be formed. This is because quartz flows plastically due to the elevation of tensile strength in the microgeometric region under the considerably small intimate pressure, even if the point is sharp. However, if the pressure increases, quartz will produce fractures, in this moment, fracture energy will be released, so that secondary flaws will not be formed until that energy is accumulated. If, in this case, the point fractures easily, the work to be done will be consumed for breaking the point, and, as a result, the material will be fractured. The shape of fractures will depend upon the radius of the point and the properties of the material. Thus, the fracture energy is insufficient to make closely-pitched secondary flaws.

In such materials as sapphire or Alundum, their fractures are large, which leads to the formation of secondary flaws independent of the apparent load, accompanied with the multiple scratching ; and this state may also be observed on surfaces polished with cerium oxide abrasives as described in section 2.4.

### 2.3.4. The Origination of Secondary Flaws during Polishing

The problem of whether the secondary flaw originates during the process of polishing or is produced by lapping is discussed.

The view that the flaw or fracture caused by lapping disappears due to the flow in polishing and reappears through etching on account of the dissolution of the polished layer has so far been most prevalent. However, as pointed out by Mitsuhashi(13) and Rawstron,(14) it is observed that latent damages appear in the direction of motion as designated.

Moreover, the fact that latent damage originates on lapped surfaces which have been etched before polishing look like the traces of their piercing into the surface obliquely through re-etching after polishing ; and that they are scattered all over the surface may be recognized during the experiments described in Section 1.3.

Therefore, it is clear that secondary flaws originate during the process of polishing.

From further consideration on this point, it may be interpreted that, since secondary flaws are originated by stress, they can be produced without abrasives as the result of the "stick to slip" phenomenon described by Kinoshita and others.(15) This effect will be greater in polishing than in lapping.

Consequently, it may be concluded that the greater part of the secondary flaws originate during polishing and that the higher degree of origination of secondary flaws on the finally polished surface with large deformation comes from the larger scratching effect.

### 2.3.5. Deformation Process of Scratched Serfaces by Etching

From the results described in the preceding paragraphs, it may be seen that the deformation process of scratched surfaces follows the same process in the generally changing stage of polished surface.

In the first place, by scratching and etching, the same effect as the Twyman effect on lapped surfaces can be seen in the state of reversion of curvature on scratched surfaces as shown in Fig. 48.

In the second place, from the curves of the degree of deformation in Fig. 49, in which the polished layers were removed from the specimens through pre-etching before scratching, it is found that the flatness improves as the scratched layers are removed, while there is no stage corresponding to the violently changing stage in polished surface.

This is caused by the removing through etching of the strains in deep parts which cannot be exposed without etching. On the other hand, near the skin, smaller numbers

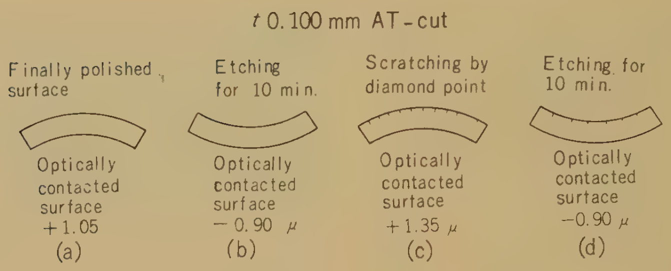

t 0.100 mm AT-cut
Finally polished surface
Etching for 10 min.
Scratching by diamond point
Etching for 10 min.
Optically contacted surface
+1.05
(a)
Optically contacted surface
−0.90 μ
(b)
Optically contacted surface
+1.35 μ
(c)
Optically contacted surface
−0.90 μ
(d)

**Fig. 48**—Reversion of curvature on scratched surface by etching.

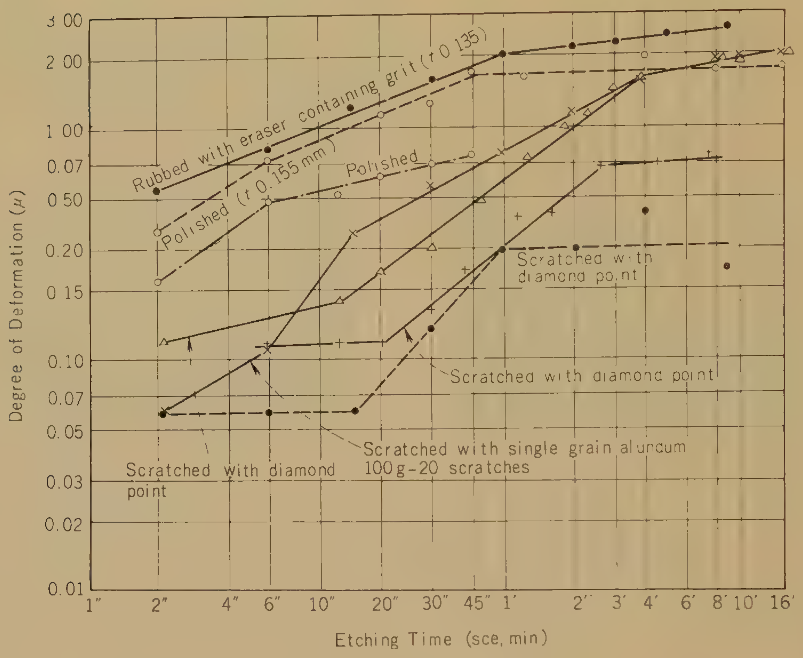


**Fig. 49**—Curves of degree of deformation on scratched surfaces.

of fractured parts are broken away from the mass where very small strains are left, so that no influence will be exercised on deformation. That is to say, in scratching, it is found that the lack of a stressed layer near the skin is shown by a flat curve and that the slower changes in the curve continues for 1 to 4 minutes.

Therefore, the origination of secondary flaws by scratching is considered to correspond to that in the gradually changing stage on polished surface. Furthermore, from Fig. 49, it is found that the first kink for a polished plate with the thickness of 0.155 mm also comes out in several seconds, almost the same as in the case of a plate with a thickness of 0.100 mm, which supports the theory that kink is determined by the degree of working and is independent of thickness. Moreover, it is noticeable that a surface rubbed by an eraser containing grit shows that it lies between the polished and scratched surfaces with respect to the deformation process because of its shallow scratches of greater numbers.

## 2.4. Sizes of Secondary Flaws in the Polished Layer

The relation of secondary flaws to the layer disturbed by polishing was obtained by measuring their depths on polished surfaces which led to the estimation of initial depths of secondary flaws before etching.

Specimens used were AT cut crystals of 14 mm dia. × 3 mm and X cut crystals of 15 mm × 14 mm × 0.0963 mm in size.

### 2.4.1. Measurement of the Size of Secondary Flaws

In AT cut crystals, the same position where secondary flaws came out was followed by the method of etching, polishing, two-beam interferometry and a dark field microscope, and the outline of the measurement is shown in Fig. 50.

After making a standard measured surface by pre-etching for 10 minutes, the whole crystals except the pre-etched parts were etched for 5, 10 and 20 minutes. After such etching, crystals were polished under definite conditions,* with the change in depth to be measured by the fringe's shift. In this measurement, flatness of the whole eighteen specimens fixed to the block was recorded in full size on the cabinet plate.

As the stock removal of polishing (0.2 $\mu$/hour) increases, the depth of the standard surface becomes smaller, and then, another part on the specimen's surface is etched to make a new standard surface. Therefore, the flatness of specimen should be carefully defined within 0.1 $\mu$.

In X cut crystals, the depth of secondary flaws was measured by means of a "Talysurf" roughness meter with magnifications of 20,000 and 50,000.

On the other hand, measurements of length and width of flaws were made by a dark field and a phase contrast microscope with magnifications of 100 to 400.

### 2.4.2. Sizes of Secondary Flaws in AT-cut Crystals

Fig. 51 shows the relation between the length and depth of secondary flaws, whose inclination is nearly at an angle of 8°30′ to the surface, from which it is clear that they have similar shapes for etching times of 5 to 20 minutes.

On the other hand, as shown in Fig. 52, the plan views of secondary flaws vary as the etching time varies, that is to say, it is recognized that the shapes for the etching time of 20 minutes are frequently found in (a) and (b), while those for the etching time of 10 minutes are found in (c), and those for the etching time of 5 minutes in (d). Further, the width along the depth does not vary at the depth of 1 $\mu$ as shown in Fig. 53.

The pitch of secondary flaws for 20 minute's etching was about 8 $\mu$ in the initial state, while it spreads to about 70 $\mu$ in the final stage, where the depth was about 2.8 $\mu$. This indicates the disappearance of about

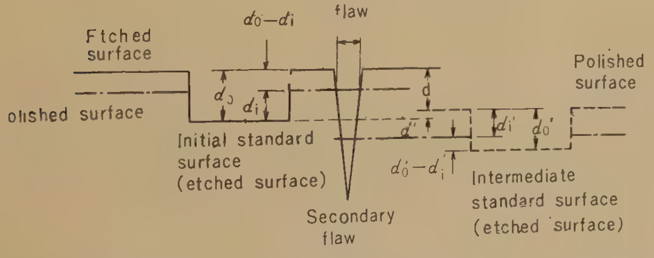


**Fig. 50**—Schematic illustration for measurement of depths of secondary flaws.

---

* Polishing pressure: 36 g/cm$^2$, revolution of a pitch polisher: 9.5 rpm, reciprocation: 40 turns/min, pitch: KR-3 (medium hardness), polishing powder: cerium oxide (Cerox).

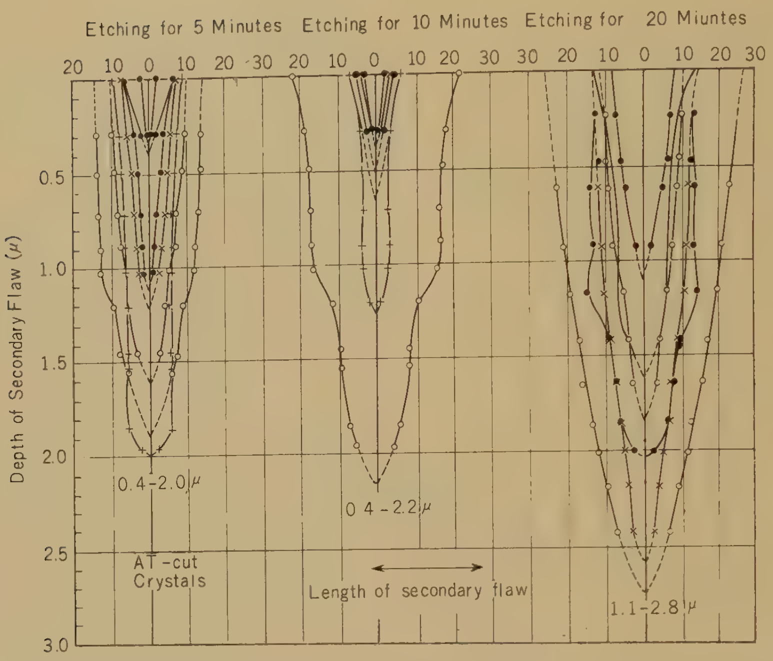


**Fig. 51**—Relation between depths and lengths of secondary flaws.

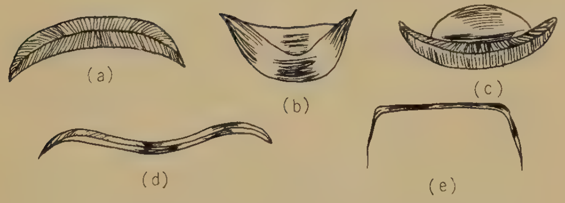


**Fig. 52**—Plan views of secondary flaws (AT-cut).

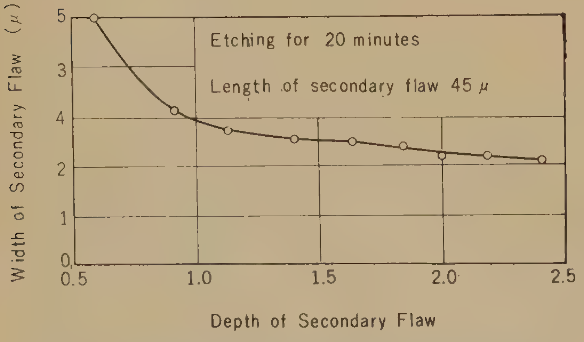


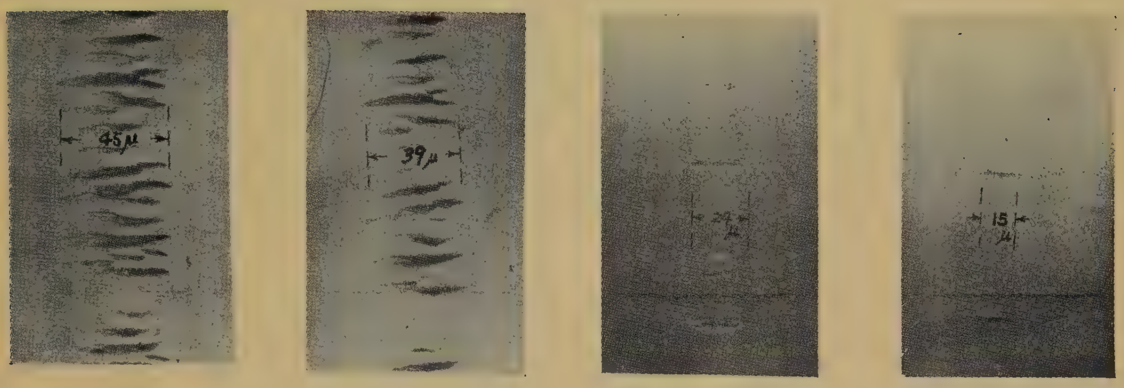
**Fig. 53**—Relation between width and depth of secondary flaws (AT-cut).

ten secondary flaws. On the other hand, in the case of a 10 minute's etching, the initial pitch of 10 μ was raised to 50 μ at the depth of 2 μ, and for the 5 minute's etching, the pitch only varied from 5 to 8 μ. In Fig. 54 the states of their disappearance are shown.

Now, from the results described above, it is assumed that the secondary flaws remaining to the last have the same conditions for their origination, and they may be classified into three grades according to there sizes. As a result, the relation of depth to etching time is indicated in Fig. 55, where depths of 0.02 to 0.65 μ is found for the etching time of 6 seconds ; that is, in the initial stage of etching, and the maximum width is found to be only 0.07 μ for the same etching time. In the case of large secondary flaws, the following relation is seen between depth $S(\mu)$ and etching time $t$ (min):

$$S=1.10\,t^{0.31}.$$

The depth of 0.02 to 0.65 μ corresponds to the etching time of 1 to 60 minutes,



(a) After Polishing for 3.5 Hours Depth 0.61 μ.

(b) After Polishing for 7.2 Hours Depth 1.16 μ.

(c) After Polishing for 12 Hours Depth 2.00 μ.

(d) After Polishing for 14.7 Hours Depth 2.42 μ.

**Fig. 54**—Disappearance of secondary flaws related to depths.

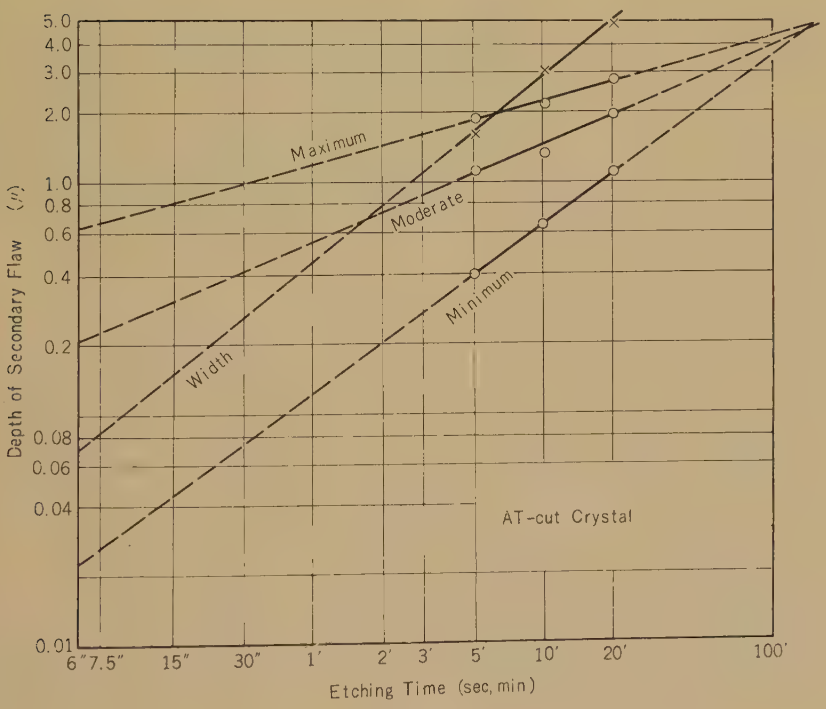


**Fig. 55**—Relation between depths of secondary flaws and etching time.

which speaks for the fact that secondary flaws play their main part in the gradually changing stage of deformation in the polished layer. The weight per one secondary flaw will be $4.4\times10^{-4}$ $\mu$g, which is $5/10^6$ of the whole removal (86 $\mu$g) of an etched plate with the diameter of 14 mm.

On the other hand, since secondary flaws are almost completely exposed between 10 and 20 minutes, the corresponding etched depth will be 1,000 to 2,000 Å, which accords on the average with the value estimated from the measured value of secondary flaws developed by etching.

Moreover, the maximum depths of secondary flaws are estimated from the roughness of etched surfaces as shown in Fig. 56, where the relation between roughness and etched depth will be found when the same etching time becomes a parameter. In this figure, roughness after 6 second's etching is found to be 0.03 $\mu$ which accords with the value measured by microgeometric interferometry. Through extrapolation of the maximum depth in the above relation, the initial depth of the secondary flaw becomes 0.95 $\mu$, which agrees with the preceding value with an error of less than 30 percent.

The result that the maximum initial depth of the secondary flaw is about 20 to 30 times as large as the roughness is quite similar to the data given by Brüche and others.(16) They reported that the depth of disturbance by scratching was 30 times as large as the depth of the scratch itself on a glass surface.

### 2.4.3. Sizes of Secondary Flaws in X-cut Crystals

Measurement was made of the depths of valleys on etched surfaces by a roughness meter, and, at the same time, etched figures were traced. Fig. 57 shows the examples recorded, while Fig. 58 illustrates the relation between etching time and maximum depth of valleys on the etched surface.

Moreover, the relation between the depth removed from the surface by etching and the depth of the valley is shown in Fig. 59, which leads clearly to the conclusion that the depth of 120 Å becomes the transition point in consideration of the change of plan views and the change of width along Z-axis as seen in Figs. 60 and 61, respectively. Namely, it can be presumed that flaws with depths up to 120 Å originate in the initial stage of secondary flaws, because the transition means the appearance of etched figures peculiar to this orientation of X cut.

This depth is, as compared with that in AT cut crystal's surface, about one half to one-fiftieth of the latter.

On the other hand, the grown depth of

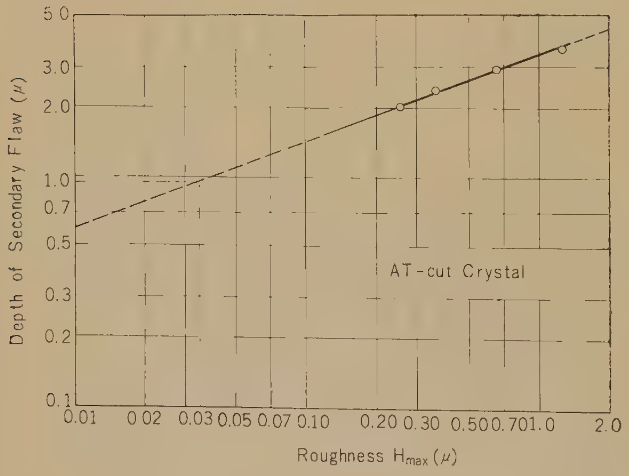
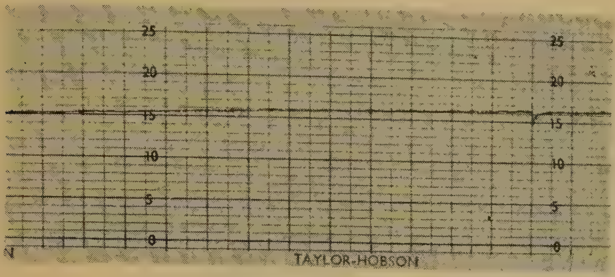
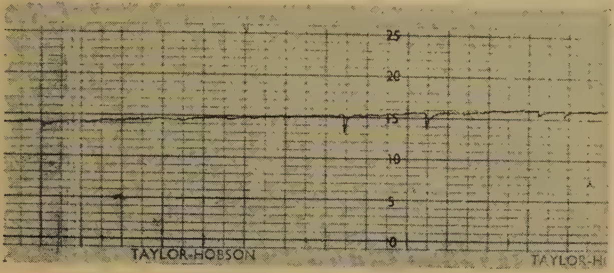


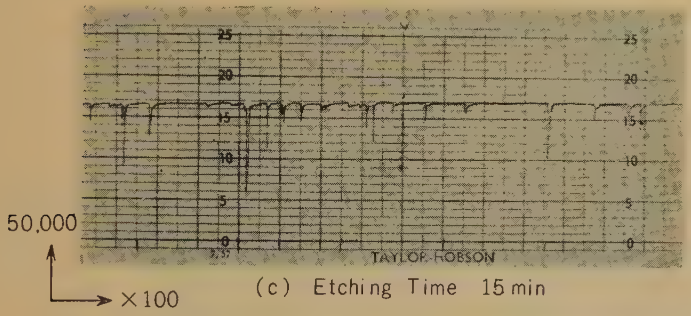
**Fig. 56**—Relation between maximum depth of secondary flaws and roughness.



(a) Etching Time 0 min



(b) Etching Time 4 min



(c) Etching Time 15 min

**Fig. 57**—Curves of depth of valleys on etched surfaces of X cut crystal (parallel to Y-direction).

the valley reaches 1,000 to 8,000 Å the same as that of AT cut crystals, and the past record of scratching, whose appearance is shown in Fig. 62, also attain the depth of several thousands of Angstroms. From these results, it can be said that a few scratching points act similarly on a polished surface regardless of their orientation.

### 2.5. Analysis of Residual Stresses

Using the result obtained in Section 2.2., an analysis of the residual stresses based on the theory of elasticity was performed.

#### 2.5.1. Fundamental of Analysis

Since quartz is an anisotropic substance, stress analysis, of course, must be treated by the general theory of anisotropic substances. However, in most X cut crystals, the deformation converted into the curvature shows its maximum deflection along the Z-axis and minimum deflection along the Y-axis; so that it can be considered that the maximum and the minimum stresses exist in such directions. Thus, the analysis in this case may be treated approximately as that of an orthotropic plate.

Therefore, the following relations are given between stress and strain.

$$\varepsilon_y = S_{22}\sigma_y + S_{23}\sigma_z$$

and

$$\varepsilon_z = S_{33}\sigma_z + S_{23}\sigma_y,$$

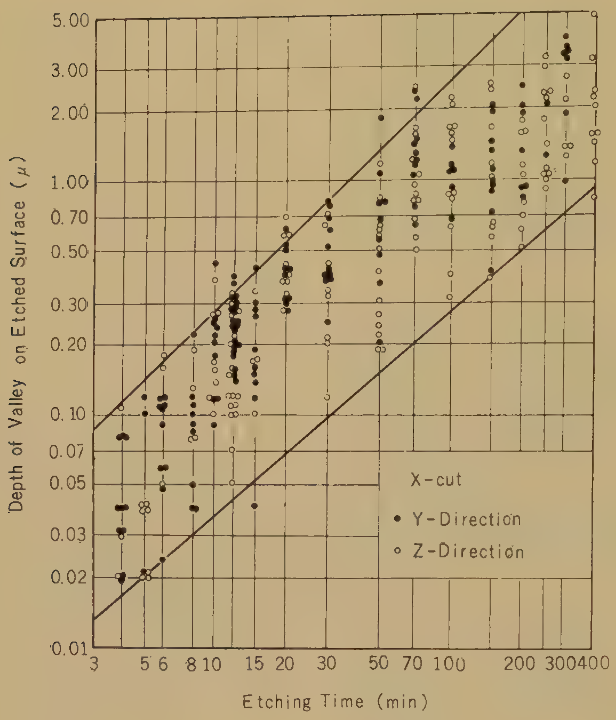


**Fig. 58**—Relation between depth of valley of etched surfaces and etching time.

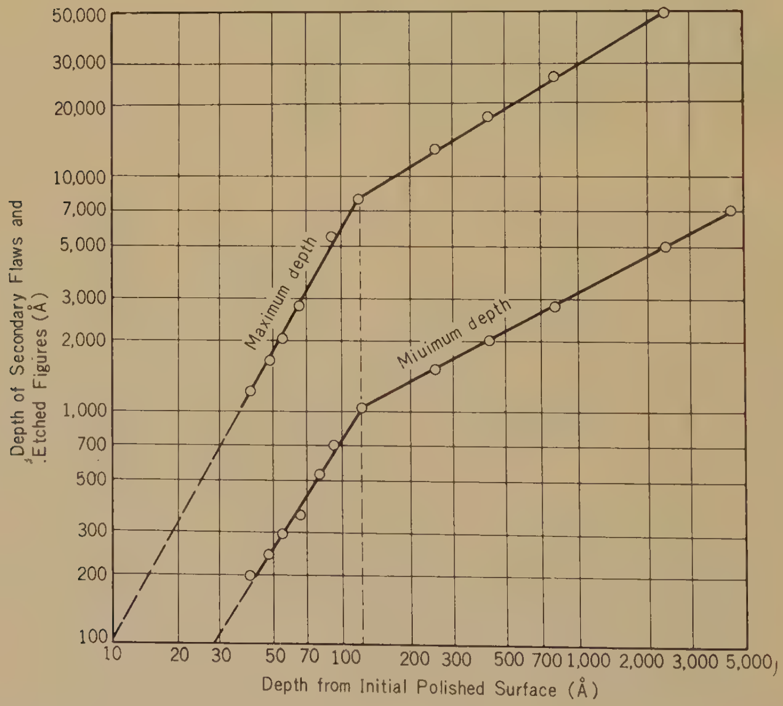


**Fig. 59**—Relation between etched depths and depth of valleys of secondary flaws.

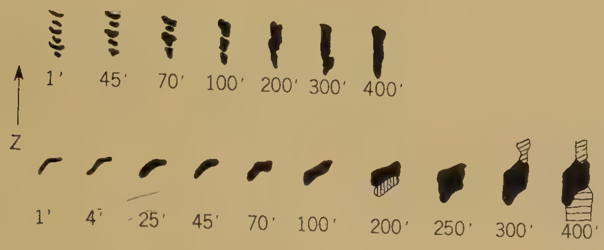


**Fig. 60**—Plan views of secondary flaws (X-cut).

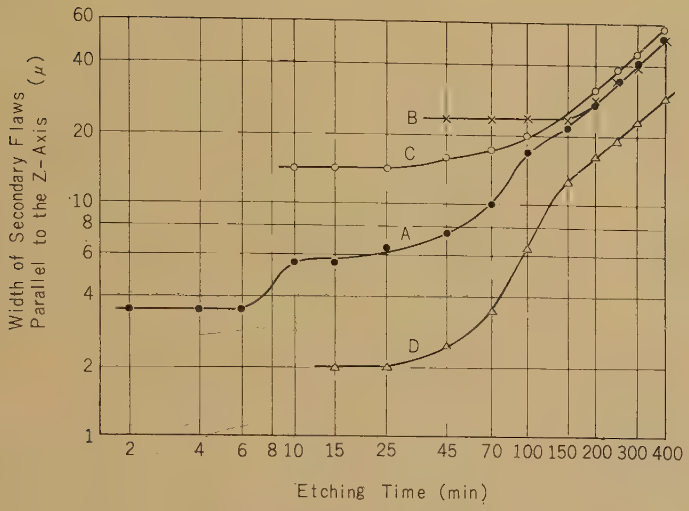


**Fig. 61**—Variation of width parallel to the Z-axis by etching.

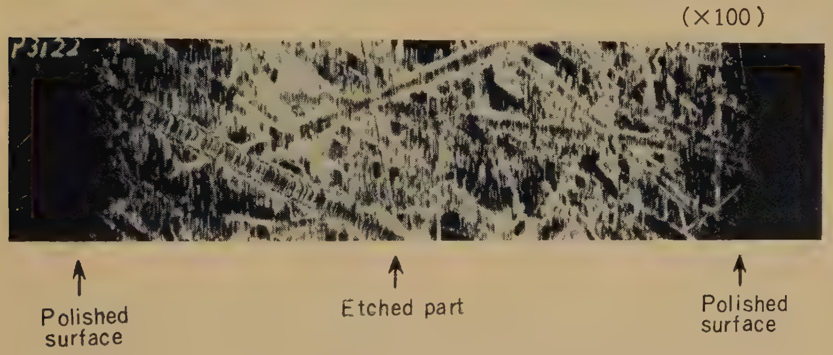


**Fig. 62**—Past records of scratching found in a deeply etched crystal.

where $\varepsilon$ is the strain, $\sigma$ stress and $S$ the elastic constant. Now in quartz, elastic constants are given as follows:(17)

$$S_{22}=S_{11}= 127.9\times10^{-14}\ \text{cm}^2/\text{dyne},$$

$$S_{23}=S_{13}=-11.0\times10^{-14}\ \text{cm}^2/\text{dyne},$$

and

$$S_{33}=95.6\times10^{-14}\ \text{cm}^2/\text{dyne}.$$

The Young's modulus and Poisson's ratio are expressed by

$$E_y=\frac{1}{S_{22}}=\frac{1}{S_{11}}=78.7\times10^{10}\ \text{dyne/cm}^2$$

$$\doteqdot 7870\ \text{kg/mm}^2,$$

$$E_z=\frac{1}{S_{33}}=104\times10^{10}\ \text{dyne/cm}^2$$

$$\fallingdotseq 10600\ \mathrm{kg/mm^2},$$

$$\nu_y = -\frac{S_{23}}{S_{22}} = -\frac{S_{13}}{S_{11}} = +0.086,$$

and

$$\nu_z = -\frac{S_{23}}{S_{33}} = -\frac{S_{13}}{S_{33}} = +0.115.$$

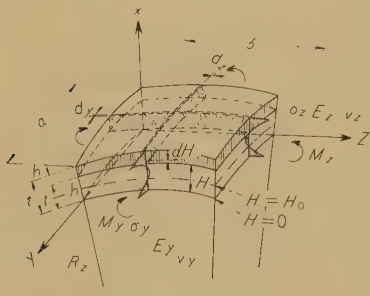


**Fig. 63**—Residual stresses in a plate.

The residual stress can be obtained by the algebraic sum of the added stresses caused by the removal of a layer of depth $h$ and the removed stress in consideration of equilibrium of bending forces and moments at the cross section (Fig. 63). By applying this to orthogonal anisotropic plate, following equations are obtained:

$$\sigma_y = \frac{E_y(t-h)^2}{6(1-\nu_y\nu_z)}\left\{\frac{d(1/R_y)}{dh} + \nu_y\cdot\frac{d(1/R_z)}{dh}\right\}$$
$$-\frac{2}{3}\cdot\frac{E_y(t-h)}{1-\nu_y\nu_z}\left(\frac{1}{R_y} + \nu_y\cdot\frac{1}{R_z}\right)$$
$$+\frac{1}{3}\cdot\frac{E_y}{1-\nu_y\nu_z}\int_0^h\left(\frac{1}{R_y} + \nu_y\cdot\frac{1}{R_z}\right)dh,$$

$\sigma_z$ can be expressed by replacing $z$ with $y$ and $y$ with $z$,

where $1/R$ is the curvature and $t$ the thickness of a plate.

In the case of a polished layer, the stressed layer is confined within the skin, which makes the second and the third terms rather negligible as compared with the first; and further, the quantity $t-h$ is approximately equal to $t$. As a result, the stresses are given as follows:

$$\sigma_y \fallingdotseq \frac{E_y\cdot t^2}{6(1-\nu_z\nu_z)}\cdot\left\{\frac{d(1/R_y)}{dh} + \nu_y\cdot\frac{d(1/R_z)}{dh}\right\}$$

$$\sigma_z \fallingdotseq \frac{E_z\cdot t^2}{6(1-\nu_y\nu_z)}\cdot\left\{\frac{d(1/R_z)}{dh} + \nu_z\cdot\frac{d(1/R_y)}{dh}\right\},$$

In AT cut crystal plates, strictly speaking, the polar coordinates should be used with the elastic constants expressed in the polar form; but taking into account the result that etching was comparatively uniform, these plates are treated as an isotropic substance. Thus the approximate mean stress is expresed as follows:

$$\sigma_m \fallingdotseq \frac{E_m\cdot t^2}{6(1-\nu_m)}\cdot\frac{d(1/R_m)}{dh},$$

where $E_m$ is taken as 7000 kg/mm², and $\nu_m$ as 0.2.

From these equations, it is clear that the stress is subjected to the differential of curvature $1/R$ to the depth $h$; which leads to a large stress in a thin deformed layer such as a polished layer, and that anisotropy is mainly emphasized in the difference between Young's moduli.

### 2.5.2. Results of Calculations

After compensating for the error of flatness by using the average flatness on both surfaces, curvatures were obtained.

Stresses calculated by making use of the equation given above are shown in Figs. 64 to 66. Conclusion derived from these results are as follows:

(1) Large compressive stresses are left over on the skin ($h=0$), whose value becomes as large as 1,000 kg/mm² for un-annealed X cut plates, 500 kg/mm² for annealed X cut plates and 70 kg/mm² for AT cut un-annealed plates, respectively.

(2) In X cut crystal plates, stress is far higher than that of AT cut crystal plate

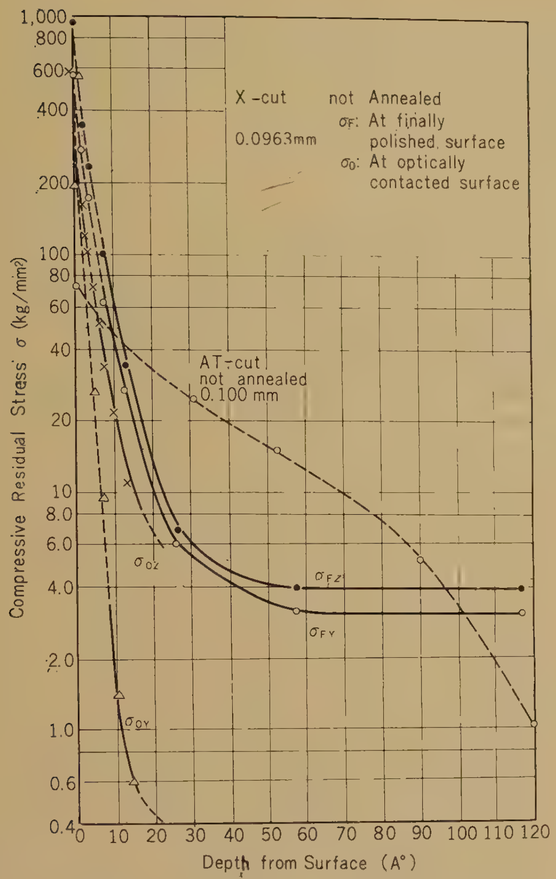


**Fig. 64**—Distribution of residual stresses in not-annealed X-cut crystals.

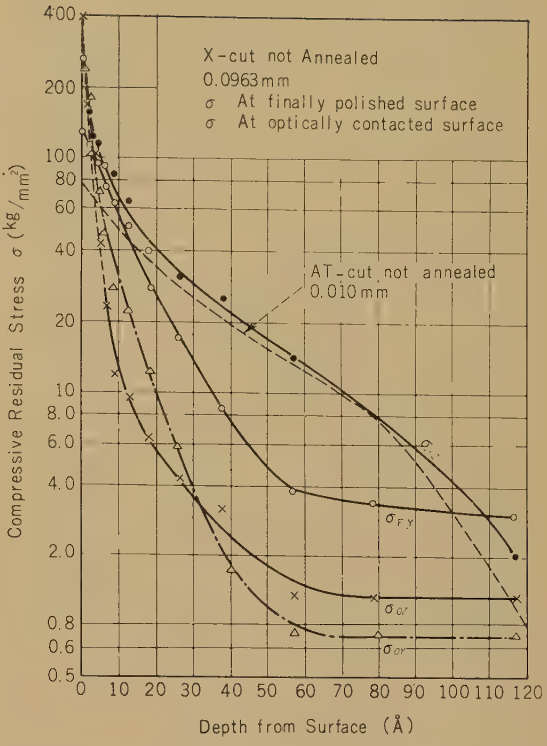


**Fig. 65**—Distribution of residual stresses in annealed X-cut crystal.

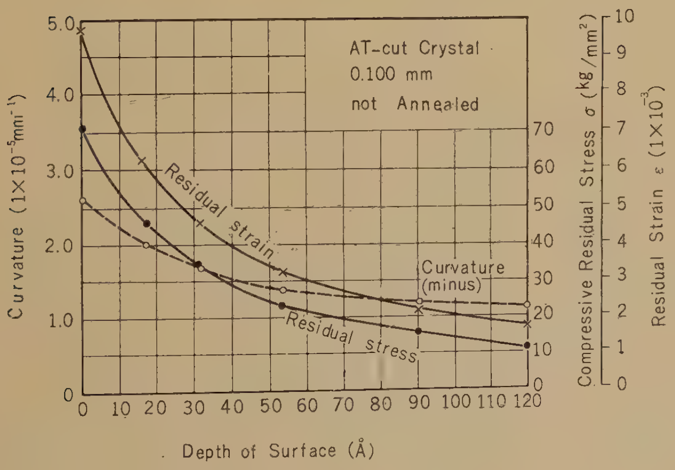


**Fig. 66**—Distribution of residual stresses in not-annealed AT-cut crystal.

because of the localized stress at the skin.

(3) $\sigma_z$ is, in general, larger than $\sigma_y$.

(4) The effect of annealing may be seen in the releasing of stress near the skin.

(5) The depth of the pure polished layer corresponds to two to four times the atomic interval along the X-axis, which is 4.903 Å, if the depth having the steepest inclination of stress is to be regarded as the polished layer.

(6) In X cut crystals, stress will, on account of a small depth of secondary flaws, be released rapidly as the depth increases ; and this tendency is different from that shown by AT cut crystals, where stress decreases gradually to the depth of about 100 Å.

On the assumption that the uniform strain appears along the direction of thickness (which means that the curvature is not a function of removed thickness), the mean strain is obtained under the condition of equilibrium of force and moment at the cross section of a plate.

Namely,

$$\varepsilon_y = \frac{4t^2}{3ha^2} \cdot F_y,$$

$$\varepsilon_z = \frac{4t^2}{3hb^2} \cdot F_z,$$

where $F$ is the maximum deflection, $h$ thickness removed until the difference between deflections is reduced to zero, $a$ and $b$ lengths of the edges, respectively ; and where $t$ the initial thickness of the plate.

In the case of an AT cut plate* (shown in Fig. 66), by substituting :

$h=2\times10^{-4}$ mm, $F\fallingdotseq 6.5\times10^{-4}$ mm, $t\fallingdotseq 1\times10^{-1}$ mm

into the above equation, the following result is obtained :

$$\varepsilon \fallingdotseq 2.4\times10^{-4}.$$

In may be seen that this value, as compared with the strain on the very thin skin ($h=0$), is about 40 times as large as the latter, which speaks for the rapid release of deformation by a slight etching, whose depth is estimated to be less than 10 Å.

### 2.6. Discussion on the Mechanism of the Polishing of Quartz

Through inquiries into the results obtained so far in the preceding sections, the cause of residual compressive stress is discussed in relation to the mechanism of quartz polishing, from which the model of the polished layer is illustrated.

#### 2.6.1. Cause of Residual Stress and the Mechanism of Polishing

The results obtained are summarized as follows :

(1) Compressive stress is left over on the polished surface ;

(2) Secondary flaws are caused by scratching, whose cause exists in tensional fracture ;

(3) Cause of origination of secondary flaws in polishing is the same as that in scratching ;

(4) In the deformation process both secondary flaws correspond with each other ;

(5) The deformation in the violent deformation stage, which is rapidly released by etching, has the same nature as that in gradual deformation stage.

From this summary, it appears necessary that the strained layer in tension be left over in order to have a compressive stress left over on the polished surface. Thus, polishing is considered to be the aggregation of micro-scratchings done by the points of abrasives during polishing, which makes the surface layer elongate along the underlayer of the plate. In this case, due to micro-scratching, plastic flow as described by Brüche and others(18) will also be produced under high pressure in microgeometric regions ; which will lead to the production of compressive stress owing to the tensional strain that makes the surface layer elongate during the coagulation process.

---

* Regarded as a square plate for simplicity.

However, when the state of polished quartz is observed by the fringes of equal chromatic order, very minute roughness seems to be left behind on the surface as the traces of micro-fractures in tension. Also Koehler(19) has already reported on the surface roughness of polished glass observed by the same fringes. Consequently, the plastic Beilby-Rayleigh layer as described by Brüche is considered to be acceptable with the consideration of its origination in the local or ideal state.

In the formation of quasi-fluid layer described by Beilby,(20) as Inoue(21) pointed out, compressive strain is to be produced on the surface layer as a result of surface tension, which will lead to the concave deformation of the plate. However, this interpretation does not agree with the experimental results already described. On the contrary, it may be explained from the results that compressive stress is left over on polished layer by micro-scratching; and it is consistent with the weaker resistance against chemical action of surface layer which is indicated in the relation between etched depth and etching time.

Further, Kamogawa(3) stated the results obtained by electron diffration showed that the polished layer was covered with an amorphous quartz layer whose atomic distribution resembled that of an evaporated quartz film, and that slope of the surface had an angle of within 30 minutes to the horizontal. In such a state of things, though the concept of flow may be formed, it will be the problem of the ratio of the surface covered with scratches and the ratio where flow has occured.

From the standpoint of the residual tensional strain, or compressive stress, it is considered that micro-scratching plays a greater part in polishing of quartz.

### 2.6.2. Model of Polished Quartz Surface

The model of polished surfaces of AT and BT cut crystals is illustrated in Fig. 67.

If the depth at which the polishing stress is released rapidly by etching, is taken as that of a polished layer, it will be about 30 Å, while the depth of secondary flaws which have influence on deformation are as great as 700 Å for AT cut and 400 Å for BT cut crystals, respectively. Moreover, for AT cut crystals, their original depth will be as large as 200–10,000 Å, and the past record of scratching to be found on deeply etched surface will be seen at the depth of about 30,000 Å.

On the other hand, in X cut crystals, the worked layer is usually shallow as compared with that of AT cut crystals as shown in

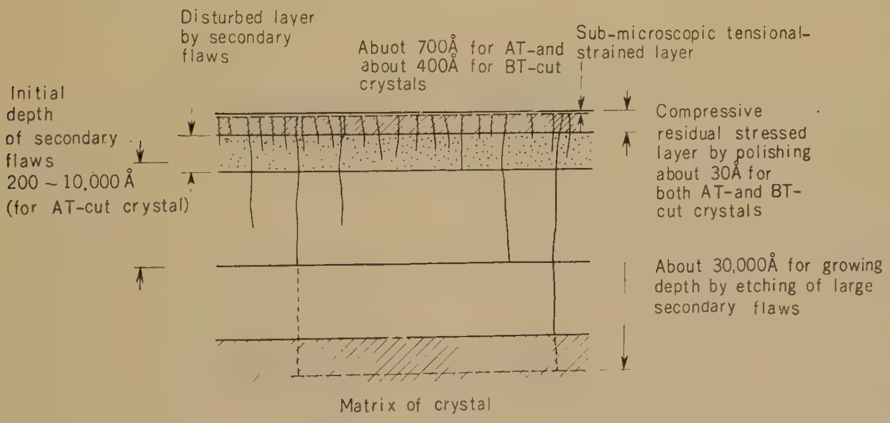

Disturbed layer by secondary flaws
Abuot 700Å for AT-and about 400Å for BT-cut crystals
Sub-microscopic tensional-strained layer
Initial depth of secondary flaws 200 ~ 10,000 Å (for AT-cut crystal)
Compressive residual stressed layer by polishing about 30Å for both AT-and BT-cut crystals
About 30,000Å for growing depth by etching of large secondary flaws
Matrix of crystal

**Fig. 67**—Sectional model of polished quartz.

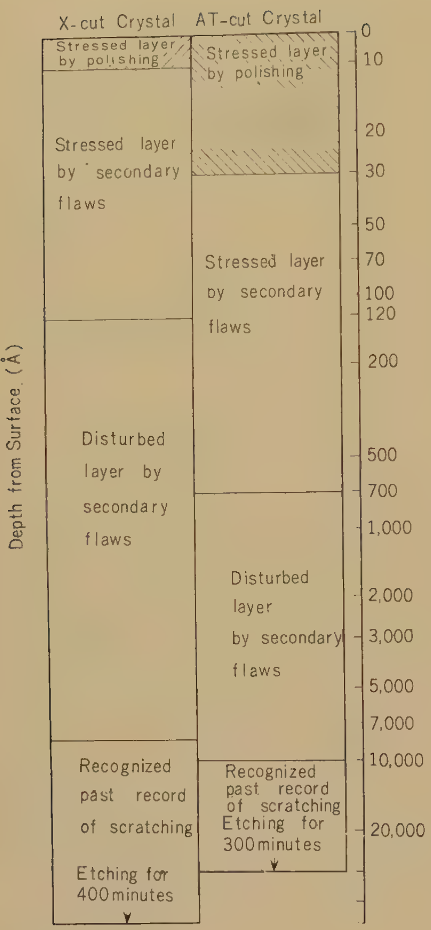

X-cut Crystal
AT-cut Crystal
Stressed layer by polishing
Stressed layer by polishing
Stressed layer by secondary flaws
Stressed layer by secondary flaws
Disturbed layer by secondary flaws
Disturbed layer by secondary flaws
Recognized past record of scratching
Etching for 400 minutes
Recognized past record of scratching
Etching for 300 minutes
Depth from Surface (Å)
0
10
20
30
50
70
100
120
200
500
700
1,000
2,000
3,000
5,000
7,000
10,000
20,000

**Fig. 68**—Comparison of the worked layer of X-cut crystal with that of AT-cut crystal.

Fig. 68 ; that is to say, a polished layer has the depth of 10 to 20 Å, while the secondary flawed layer has the depth of within 120 Å at the time of its origination. This may be because of the close arrangement of atoms in X cut crystals. However, the depth of scratched trace whose past record is found in deeply etched surface is almost the same as that of AT cut crystals.

### 2.7. Summary

The nature of polished quartz surfaces was investigated from the standpoints of the residual stress and the deformation of the plate. This may be summarized as follows :

(1) By direct measurements of etched depth, in which the key point was the use of the fringes of equal chromatic order, it was found that the skin of polished surfaces were dissolved easily, and the relation of etched depth to etching time was obtained as follows:

$$h=K\cdot t^{\alpha},$$

where $K$ and $\alpha$ are constants to be determined by orientation. The rate of etching was greatest for AT cut, next for BT cut, and least for X cut crystals.

(2) From the process of deformation of the polished surface by etching, it was indicated that worked layers might be classified into three types, and it was also concluded that compressive stress was left over on the surface due to the relation of the curvature change during the deformation process.

(3) By the scale model test of scratching, it was clarified that secondary flaws originated from the stress in tension along the radial direction of contact circles produced by points of abrasives situated behind the direction of scratching.

Furthermore, by comparison of both deformation processes with each other, it was shown that the secondary flaws originated by scratching corresponded to those produced by polishing.

(4) Since the sizes of secondary flaws were measured with respect to polished layer, the initial depth before etching was estimated at 200 to 10,000 Å for AT, and at about 120 Å for X cut crystals, respectively.

(5) It was clarified that a compressive stress, whose order was 1,000 kg/mm$^2$ for un-annealed X cut, 500 kg/mm$^2$ for annealed X cut and 70 kg/mm$^2$ for un-annealed AT cut crystals, respectively, was left over on the skin, as was seen from the analysis of residual stress.

(6) From the standpoints of the stress and deformation, it is considered that the

mechanism of quartz polishing comes from the aggregation of micro-scratchings by points of abrasives including plastic flow.

(7) A model of polished quartz surface was illustrated from the results obtained in this study.

## Conclusion

These studies described thus far were concerned with the development of a polishing technique for VHF crystals units in the first place, and with the clarification of mechanism of quartz polishing from the viewpoint of deformation and residual stress in the second place.

It may be concluded as follows :

(1) The working method, process and precise measuring method for quartz plates with the thickness of 35 $\mu$ and the working accuracy of the order of 0.1 $\mu$ were studied. As a result, polishing techniques for VHF crystal units whose frepuency is as high as 140 Mc/s has been established.

(2) Deformation of thin polished quartz plates was noticed, and, as a result, the nature of residual stress, stages of worked layers and their depths were clarified, with residual stress having been analyzed at the same time. This led to a conclusion that the mechanism of polishing quartz was considered to be the aggregation of micro-scratchings. In addition, the model of polished quartz surface was given in relation to the depth of worked layers, which may suggest the mechanical factors affecting the vibration loss of crystal units in higher frequency range.

## Acknowledgement

The authors are indebted to Dr. M. Ōkoshi and Dr. N. Takagi of the Tokyo University for their valuable advice and encouragement, and to Dr. K. Takahara of this laboratory for his helpful suggestions.

## References

(1) K. Takahara, "Researches on the Development of Quartz Crystals Units," *Electr. Comm. Labor. Tech. Journ.*, N.T.T., **8**, 2, p. 123, 1959 (In Japanese) and Rev. of Electr. Comm. Labor., N.T.T., in press.

(2) F. Twyman, Prism and Lens Making, 2nd. ed., p. 171, 1952, Hilgers & Watts Ltd. Co., London.

(3) H. Kamogawa, "Study on Structure of Polished Quartz Surfaces by Electron Diffraction," Journ. of the Physico-Mathematical Soc. of Japan, **17**, 8, p. 384, 1943. (in Japanese).

(4) E. A. Gerber, "VHF Crystal Grinding," *Electronics*, **27**, 3, p. 161, 1954.

(5) I. Ida & Y. Arai, "Development of Lapping for Quartz Oscillator-Plates," *Reports of Electr. Comm. Labor.*, N.T.T., **6**, 1, p. 12, 1958.

(6) Lord Rayleigh, "A Study of Glass Surface in Optical Contact," *Proc. Roy. Soc.*, **A156**, 888, p. 326, 1936.

(7) J. Rumsay, "The Effect of Eccentric Loading of Optical Flat during Grinding or Polishing," *J.S.I.*, **32**, 9, p. 338, 1955.

(8) S. Tolansky, Multiple Beam Interferometry of Surfaces and Films, 2nd. ed., p. 96, 1949, Oxford at the Clarendon Press, London.

(9) F. Twyman, *ibid.*, p. 318,

(10) C. J. Köester, "Phase Shift Effect in Fringes of Equal Chromatic Order," *J.O.S.A.*, **48**, 4, p. 255, 1958.

(11) K. Natsume and K. Kinoshita, "Experimental Studies on 'Stains' Formed on Polished Surface of Optical Glasses, III Geometry of Stained Area," *J. of Appl. Phys, Japan*, **28**, 3, p. 132, 1959. (in Japanese).

(12) S. Timoshenko, Theory of Elasticity, 1st. ed., p. 339, 1934, McGraw-Hill, N. Y.

(13) G. Mitsuhashi, "Studies on the Polishing of Optical Glasses (II) Latent Damages and Hardness of Asphalt," *Journ. of Appl. Phys. Japan*, **13**, 9, p. 288, 1944. (in Japanese).

(14) G. O. Rawstron, "The Nature of Polished Glass Surfaces," *Journ. of the Soc. of Glass Technol.*, XLII, 209, p. 253T, 1958.

(15) K. Kinoshita & others, "Friction Tracks Produced when Glass Slides," *Journ. of Appl. Phys. Japan*, **24**, 6, p. 244, 1955. (in Japanese).

(16) E. Brüche & K. Peter, "Das Polieren von Glas Teil V: Kompression und Plastizität von Glas," *Glastechn. Ber.*, **32**, 9, s. 341, 1958.

(17) W. G. Cady, Piezoelasticity, 1st. ed., p. 137, 1946, McGraw-Hill, N.Y.

(18) E. Brüche & H. Poppa, "Zur Frage der Rayleigh-Beilby Schicht bei Glas," *Z. für*

*angew. Phy.*, **8**, 10, s. 486, 1956.

(19) W. F. Koehler, "Multiple Beam Interference Fringes of Equal Chromatic Order," Part II & VII: Polishing Mechanism of Glass, *J.O.S.A.*, **43**, 9, p. 743, 1953 and **45**, 12, p. 1015, 1955.

(20) G. Beilby, Aggregations and Flows of Solids, 1st. ed., p. 114, 1921, MacMillan & Co. Ltd., London.

(21) K. Inoue, "Deformation of Glass Plate by Wearing and Structure of Worn Glass Surface (2) Deformation of Glass Plate by Polishing and Chemical Action and Structure of Polished Glass Surface." *Journ. of Appl. Phys. Japan*, **28**, 2, p. 71, 1959. (in Japanese).

* * * *

681. 142:511. 122

# High Speed Adding System*

*Noriyosi KUROYANAGI*†

*Using Boolean algebra, the author has extracted the propagating function of the carry signal from the other adding functions of an electric computer, and described that function. The logical function is performed during the period of one step of the clock pulse, using a carrier propagating circuit which consists of transistors, diodes and pulse transformers. The essential part of the propagating circuit is composed of series and parallel connections of transistors which are used as gate elements.*

*Logical pulse output obtained by a simple logical treatment of every bit of addend and the corresponding bit of the augend is sent into the carrier propagating circuit, where special gates pass into the conductive state, and closed circuits are formed. These closed circuits can produce the carry signal of each bit instantly and simultaneously.*

*The author has confirmed the possibility of a remarkable increase in adding speed. First a circuit suitable for binary addition is explained, and then a circuit suitable for the dicimal system is shown. Taking into consideration the necessary number of bits for scientific calculation, a carrier propagating circuit with forty bits was constructed. It shows good dynamic characteristics.*

## Introduction

The calculating speed of an electric computer depends mainly on the speed of the adder which is one of the main parts of the arithmetic equipment. Adding speed of a parallel adder is restricted by the propagating time of the carry signals. In an AC pulse system composed of diode logics, direct connection of logical operational circuits (i.e.,logics) over many stages is impossible, since the input signal power is attenuated while passing through them. Accordingly, after the output signal power passes through two or three stages of logics, it is always amplified before it is sent into the next stage. However, as the regenerative amplification of the output necessarily involves a time delay, in actual regenerative amplifiers a delay equal to about one cycle of the clock pulse takes place between the input and the output signals.

Therefore, for adding binary numbers of $n$ bits, if we use the method in which we start the addition at the least significant digit, add the carry output produced there to the addition at the next digit, and repeat this process on to the most significant digit at least $n$ stages of regenerative amplification; that is, $n$ steps of logical operation are necessary to propagate carry signals from the lowest to the $(n+1)$th bit. The larger the number of bits is, the longer the necessary time for addition by this method will be.

A new logical circuit, which is explained in this report, has been designed to shorten the time for addition considerably, by obtaining the carries of all digits at one time (i.e., by a one step operation).

Among other high speed carry circuits, there is a parametron circuit, and the circuit used in the SEAC and DYSEAC electronic computers of the United States Bureau of Standards (NBS). However the

---

* MS in Japanese received by the Electrical Communication Laboratory, Feb. 24, 1960. Originally published in *The Journal of the Institute of Electrical Communication Engineers of Japan*, Vol. 42, No. 11, pp. 1051–1057.

† Sakurai's Research Section.

latter is rather uneconomical, because it takes comparatively long to dispose of carries and requires gigantic logical elements.

### 1. Description of the Adding Function

The augent and the addend of a binary number of $n$ bits are denoted by

$$X=\sum_{\nu=1}^{n} X_\nu \cdot 2^{\nu-1},$$

$$Y=\sum_{\nu=1}^{n} Y_\nu \cdot 2^{\nu-1}$$

respectively, and their sum by

$$Z=\sum_{\nu=1}^{n+1} Z_\nu \cdot 2^{\nu-1}.$$

Where $X_\nu$, $Y_\nu$ and $Z_\nu$ are binary logical values (i.e., either 0 or 1). Basically, the adding function is described as follows, beginning with the least significant digit:

$$\left.\begin{aligned}
&Z_1=X_1 \oplus Y_1 \quad \text{Putting} && V_2 \equiv X_1 \cdot Y_1\\
&Z_2=V_2(X_2 \cdot Y_2 \oplus \overline{X_2} \cdot \overline{Y_2}) && V_3 \equiv V_2(X_2 \oplus Y_2)\\
&\qquad +\bar{V}_2(X_2+Y_2) && \qquad +X_2 \cdot Y_2\\
&Z_3=V_3(X_3 \cdot Y_3 \oplus \overline{X_3} \cdot \overline{Y_3}) && V_4 \equiv V_3(V_3 \oplus Y_3)\\
&\qquad +\bar{V}_3(X_3+Y_3) && \qquad +X_3 \cdot Y_3\\
&\vdots\\
&Z_\nu=V_\nu(X_\nu \cdot Y_\nu \oplus \overline{X_\nu} \cdot \overline{Y_\nu}) && V_{\nu+1} \equiv V_\nu(X_\nu \oplus Y_\nu)\\
&\qquad +\bar{V}_\nu(X_\nu+Y_\nu) && \qquad +X_\nu \cdot Y_\nu\\
&\vdots\\
&Z_n=V_n(X_n \cdot Y_n \oplus X_n \cdot Y_n) && V_{n=1} \equiv V_n(X_n \oplus Y_{n,})\\
&\qquad +\bar{V}_n(X_n+Y_n) && \qquad +X_n \cdot Y_n\\
&Z_{n+1}=V_{n+1}
\end{aligned}\right\} \quad (1)$$

where $\oplus$ represents addition in modulus 2.

If we introduce the logical value $V$ which stands for the carry function, a simple method of description such as Eq. (1) is possible. If we use Eq. (2) in which $C_\nu$ and $S_\nu$ stand for the carry and sum derived from $X$ and $Y$ for each digit, and $\overline{S}_\nu$ stands for the negative of bit $S_\nu$, then:

$$\left.\begin{aligned}
&C_\nu=X_\nu \cdot Y_\nu\\
&S_\nu=X_\nu \oplus Y_\nu, \quad \overline{S}_\nu=X_\nu \cdot Y_\nu+\overline{X}_\nu \cdot \overline{Y}_\nu.
\end{aligned}\right\} \quad (2)$$

and Eq. (1) can be simplified to:

$$(Z)\quad \left.\begin{aligned}
&Z_1=S_1\\
&Z_2=V_2 \cdot \overline{S_2}+\overline{V_2} \cdot S_2=V_2+S_2\\
&\vdots\\
&Z_\nu=V_\nu+S_\nu\\
&\vdots\\
&Z_n=V_n+S_n\\
&Z_{n+1}=V_{n+1}
\end{aligned}\right\} \quad (3)$$

$$(V)\quad \left.\begin{aligned}
&V_2=C_1\\
&V_3=V_2S_2+C_2\\
&\vdots\\
&V_\nu=V_{\nu-1}S_{\nu-1}+C_{\nu-1}\\
&\vdots\\
&V_n=V_{n-1}S_{n-1}+C_{n-1}\\
&V_{n+1}=V_n \cdot S_n+C_n.
\end{aligned}\right\} \quad (4)$$

Consequently, if we know the logical function $V$, sum $Z$ can be easily obtained by the operation in each bit. From the 10 digit binary numbers $X$ and $Y$ shown in Table 1, $Z$ can be found by the method to be described.

$S$ and $C$ can be obtained from $X$ and $Y$ of Equation (2), and are listed in Table 1. From the Equation (4), we can find the following relations: if $C_\nu$ is 1, $S_{\nu+1}$, $S_{\nu+2}$, $\cdots\cdots\cdots$ and $S_{\nu'}$ are all 1 (where $\nu' \geq \nu$), and $S_{\nu'+1}=0$, then $V_\nu$, $V_{\nu+1}$, $V_{\nu+2}$, $\cdots\cdots\cdots$ and $V_{\nu'+1}$ are all 1, and the values of other $V$ are 0. The logical values of $S$ and $C$ which make the logical values of $V$ one are connected by the dotted lines in Table 1. Since $C_\nu \cdot S_\nu=0$ from the relations in Equation (2), duplication of such dotted lines cannot take

**Table 1**

EXAMPLES OF ADDING FUNCTION $(Z=X+Y)$

| $\nu$ | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $X$ | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| $Y$ | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| $S$ | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| $C$ | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| $V$ | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| $Z$ | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |

place. $Z_\nu$ is obtained by inversion of the logical value of $S_\nu$ (i.e., if $S_\nu=1$, $Z_\nu=0$, and if $S_\nu=0$, $Z_\nu=1$) where $V_\nu$ is 1, and by transferring the value of $S_\nu$ where $V_\nu$ is 0. $V$ is called the inverting signals.

## 2. Construction of Circuits

### 2.1. Outline

Fig. 1 illustrates the block diagram which performs the adding function shown by Equations (2), (3), and (4).

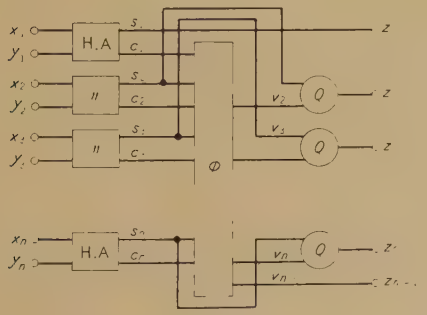


**Fig. 1**—Block diagram of parallel birary adder.

In the illustration of the input and output lines of each block circuit, $X_1$ denotes the line carrying the signal input corresponding to the logical value $X_1$. The half adder (H.A.) which can obtain from $X_\nu$ and $Y_\nu$ the carry output $C_\nu$ and the sum output $S_\nu$ (and also $\bar{S}_\nu$, but $S_\nu$ omitted in this diagram). $\Phi$ is the carry propagating circuit, which can obtain all the values of inverting signals from $C$ and $S$ (and $\bar{S}$) simultaneously. $Q$ is the exclusive $OR$ circuit, which carries out the operation of addition in modulus 2 and obtains $Z_\nu$ by inverting $S_\nu$ according to the value of $V_\nu$.

By adding input signals to all the input terminals of $X_\nu$ and $Y_\nu$ at the same time, all the output signals can be obtained at all the output terminals of $Z_\nu$ simultaneously. To compensate for the attenuation of the logical operation, it is sufficient to insert a pulse regenerative amplifier after the half adder, after the carry propagating circuit, and after the exclusive $OR$ circuit. Therefore three time steps are sufficient for addition.

In the circuits in the present discussion, the $AC$ (dynamic) system, which is synchronized with the clock pulse and which makes the existence and absence of a pulse correspond respectively to the binary logical values 1 and 0 is used.

### 2.2. The Half Adder (H.A.)

The circuit to obtain the pulse outputs that correspond to $C_\nu$, $S_\nu$, and $\bar{S}_\nu$ from the pulse inputs that correspond to the logical values of $X_\nu$ and $Y_\nu$; that is, the circuit to carry out the logical operation expressed by Equation (2), can be easily constructed by using diode logic, as shown in the Fig. 2. It is assumed that the regenerative amplifier of the previous stage, which supplies the pulse inputs $X_\nu$ and $Y_\nu$ to the H.A., can also supply the pulse inputs $\bar{X}_\nu$ and $\bar{Y}_\nu$ at the same time.

The exclusive $OR$ circuit performs the function of the half adder only partially, and it consists of the parts necessary for getting the outputs for $S$ in the Fig. 2.

### 2.3. The Carry Propagating circuit ($\Phi$)

The carry propagating circuit $\Phi$ is the

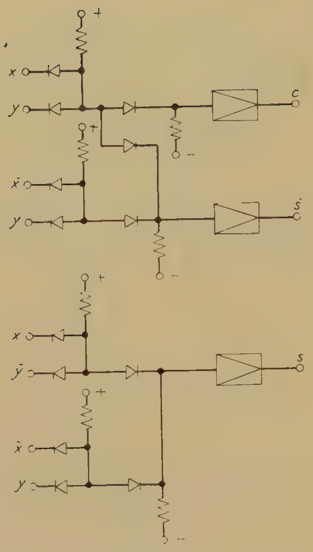
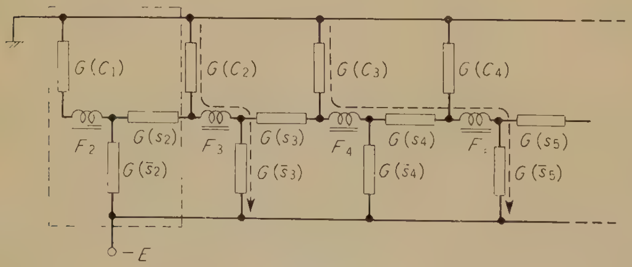


**Fig. 2**—Circuit of half adder.

central part of this adder, and determines the adding speed. The circuit structure is illustrated in Fig. 3 (a) using two terminal "black boxes" for the gate elements. $G(C_\nu)$, $G(S_\nu)$, and $G(\bar{S}_\nu)$ are the gate elements driven by the pulse inputs that correspond to $C_\nu$, $S_\nu$, and $\bar{S}_\nu$ respectively. $F$ is a pulse transformer. The gate element driven by the pulse input for the logical value 1 conducts only during the period while the input pulse continues. The non-driven gate element for the logical value 0 is held in a non-conductive state.

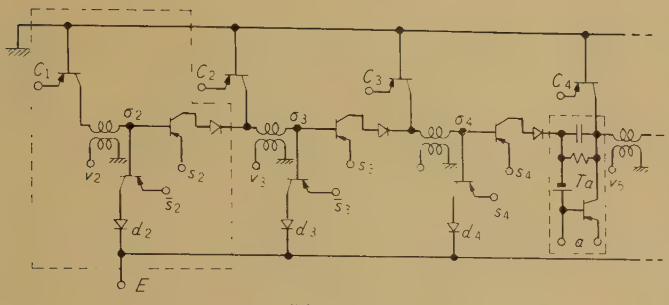
For the condition that the pulse inputs for the first through the fifth $C$ and $S$ lines shown in Table 1 drive the corresponding gate elements, the connective circuits formed by connecting gate elements held in the conductive state are indicated by the dotted lines in Fig. 3 (a). Therefore, the current flow into these circuits will send the corresponding signal output for $V$ through the pulse transformers $F$ which are inserted in these circuits.

The explanation of the circuit function in general terms is as follows: if all the values of $C_\nu$ are 0, all the values of $V_\nu$ are also 0, because no connective circuit can be formed in this case; if $C_\nu=1$, the corresponding gate element $G(C_\nu)$ will become conductive. What would happen in the next bit $(\nu+1)$ is: (i) if $S_\nu+1=0$, $G(S_\nu)$, and $G(S_\nu+1)$ are held in the non-conductive state, the circuit $G(C_\nu)-G(\overline{S_\nu+1})$ will be formed, and the pulse output will be obtained throngh the pulse transformer $F_\nu+1$; and (ii), if $S_\nu+1=1$ and $S_\nu+2=0$, $G(S_\nu)$, $G(S_\nu+1)$, and $G(S_\nu+2)$ are held in the non-conductive state, the connective circuit $G(C_\nu)-G(S_\nu+1)-G(\overline{S_\nu+2})$ will be formed, and the pulse outputs will be obtained through $F_\nu+1$ and $F_\nu+2$. In other words, the connective circuit begins from $G(C_\nu)$ and extends to the gate element $G(\overline{S_\nu+h})$ at the $(\nu+h)$ th bit, where the value of $S$ line changes from 0 to 1 for the first time after the $\nu$ th bit. Here $h$ is defined as the length of the connective circuit. $h$ can take the values 1, 2, etc. Since the pulse output is obtained through $h$ pulse transformers $(F_\nu+1, F_\nu+2, \cdots\cdots F_{\nu+}h)$ which are inserted in the connective circuit, the logical function that was defined by Equation (4) may be



(a) Φ (I)

**Fig. 3 (a)**—Propagating circuit of carry signal, ( I ) and ( II ).



(b) $\Phi$ (Ⅱ)

**Fig. 3 (b)**—Propagating circuit of carry signal, (Ⅰ) and (Ⅱ).

accomplished with precision.

Moreover, it is possible to give the logical inputs to all the input terminals at one time, and to obtain the necessary logical outputs at all the output terminals simultaneously.

Fig. 3 (b) illustrates a circuit in which transistors are used as gate elements. Pulse inputs for $C_\nu$, $S_\nu$, and $\bar{S}_\nu$ are applied to input terminals $c_\nu$, $(s_\nu\sigma_\nu)$, and $(\overline{s_\nu\sigma_\nu})$ respectively. When the transistor is driven by the pulse input, emitter current $I_e$ flows only during the time of the pulse width $\tau$ sec. Therefore if the voltage difference between the collector and the base is maintained at a suitable value, a current pulse $\alpha I_e$ can flow in the collector circuit. That is to say, the transistor passes into the conductive state. On the other hand, in transistors to which the pulse input has not been applied emitter current cannot flow. Accordingly almost no collector current can flow in them. As a result, a high resistance appears between their collector and base. This means that they are held in the non-conductive state.

Diodes are inserted in this circuit to determined the direction of the currents in a precise manner. The circuit $\Phi$ is an iterative circuit. It consists of a cascade connection of unit circuits, which are indicated by the parts enclosed by the dotted lines in the Fig. 3 (b). Each of the unit circuits consists of three transistors, corresponding to one input bit.

## 2.4. Dynamic Characteristics of $\Phi$

We should consider that the maximum scale of the numbers treated by the present binary electric computer is at least forty bits. Therefore we should be able to construct a propagating circuit by a cascade connection of forty unit circuits. However, it is not easy to make such a multiple stage cascade circuit from the elements now available, and to expect good dynamic characteristics from it. The following is the author's considerations on the dynamic characteristics of $\Phi$.

### (*1*) *The Fluctuation of the Logical Output* (*V*)

The longer the length $h$ of a connective circuit is; the lower the pulse output is in general. This phenomenon is caused by the fact that the voltage which is across each transistor held in the conductive state, decreases with the increase of $h$, and finally its polarity becomes inverted. For the condition that $R$ stands for the load resistance of each transistor, and that $E_c$ stands for the voltage between the collector and the base of each transistor,

$$E_c=(-E+h\cdot\alpha I_e\cdot R)/(h+1). \qquad (5)$$

Fig. 4 shows the static characteristics of a grounded base transistor circuit. On the assumption that $R=70\,\Omega$, which includes the diode resistance and the output resistance viewed, the characteristics in the cases when $E_c$ takes the values of $-2$ V, $-1$ V, and 0 V are shown by the curves $1_1$, $1_2$, and $1_3$ respectively.

These curves show that the collector current suddenly decreases when $E_c$ de-

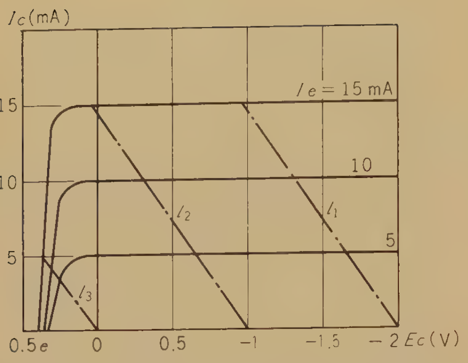


**Fig. 4**—Static characteristics of grounded base circuit.

creases to lower than a certain value. This decrease tendency is caused by the equivalent resistance of the diode, which increases with the decrease of the collector current. The decrease of the collector current means the decrease of $\alpha$. In order to avoid this undesirable effect, it is helpful to increase the absolute value of the power-supply voltage, but this method is not only limited by the maximum voltage rating of the transistors used, but also the output pulse amplitude varies widely with the change of the length of $h$. It is also effective to decrease the value of the output resistance viewed through the transformer, but this method has the defect of decreasing the signal output.

### (2) *Increase of the Voltage Across the Transistor*

Let us assume that an open connective circuit with the length $k$ is formed when $C_\nu = S_\nu = 0$, $S_{\nu+1} = S_{\nu+2} = \cdots\cdots\cdots = S_{\nu+k-1} = 1$, and $S_{\nu+k} = 0$. (If $C_\nu = 1$, a connective circuit with the length $h = k$ is formed.) The $e_0$ in the Fig. 4 denotes the voltage existing between the collector and the base of the transistor which cannot conduct collector current even if the pulse input ($I_e = 5$ mA) is applied to it. Therefore, if we indicate by $E_k$ the voltage across the transistor $T(C_\nu)$, (this symbol is meant to stand for the transistor in Fig. 4 which corresponds to the gate element $G(C_\nu)$ in Fig. 3,) $E_k$ is given as follows from the equivalent circuit of Fig. 5:

$$E_k = -E - ke_0. \qquad (6)$$

Therefore, we should consider that the value of $E_k$ will not exceed the maximum voltage rating of the transistor.

### (3) *The Accumulation of Leakage Current*

It is not desirable for any leakage current to flow the open connective circuit. In actuality, however, there are some such currents, which are illustrated with dotted lines in Fig. 5. As a result, small pulse outputs are observed through the pulse transformers. The currents accumulate with the increase of $k$ until they increase to a value that cannot be neglected. The leakage currents consist of the currents which flow through the capacity† and back resistance‡ of transistors $T(S_\nu)$, $T(C_\nu)$, $T(C_{\nu+1})$, ········ $T(C_{\nu+k-1})$, and the currents which flow through the capacity and back resistance of

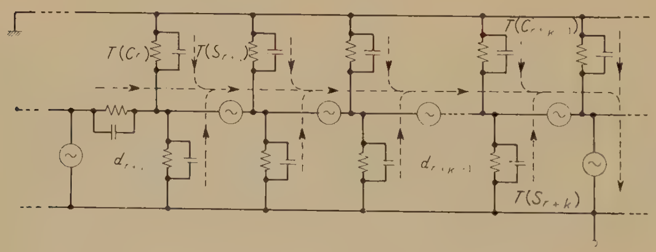


**Fig. 5**—Leakage current paths.

---

† Collector capacity.

‡ The back resistance corresponds to $I_{co}$ that is defined as the collector current which flows in the transistor with no emitter current.

diodes $d_{\nu+1}$, $d_{\nu+2}$, ········$p_{\nu+k-1}$. The leakage effect caused by the capacity of the diodes is especially large.

(4) *The Phase Shift between the Input and the Output Signals*

The value of the phase shift is determined by the phase characteristic of $\alpha$ of the transistor, and by the phase characteristics of the pulse transformer. Therefore, it is desirable to use the elements whose characteristics are satisfactory at the clock pulse repetition frequency.

(5) *Desirable Characteristics for the Transistors to be Used*

Because the forward resistance of the diode is larger for a small input than for a large input, it is effective to flow a stronger current which is selected in the closed connective circuit. Since the transistors are used in grounded base circuits, there will be no problem of delay caused by saturation.

In the case of the connective circuit, the power which is dissipated by the transistor is comparatively small. Although the current flowing in it is large, the voltage across the transistor is very small.

Therefore, it is desirable to use transistors which can handle large collector currents, but it is not necessary for the collector dissipation rating to be large. It is also desirable that the capacity and the current of the collector of the transistor when no emitter current flows be kept as small as possible, based upon the reason stated in (3) of this section.

### 2.5. Attaching Circuits

To avoid the undesirable dynamic characteristics of $\Phi$, it is necessary to use elements with superior characteristics, but it is also effective to use the following circuit as some countermeasures:

(1) *Power-Supply Circuits*

These circuits are indicated by the parts enclosed with dotted lines in the Fig. 3 (b). The capacitor $K$ is charged when $\Phi$ is not driven. The voltage across the capacitor is used as a part of the source voltage, when the branch circuit containing the capacitor becomes a part of the connective circuit, which has been formed selectively by the input pulses. In other words, the pulse input is applied to terminal during interval of successive clock pulses, and drives the transistor $T_a$ so as to give $K$ a charge over a certain fixed value constantly. Ta is held non-conductive while $\Phi$ is not being driven.

Insertion of pulse transformer $F_a$ serves to separate the power-supply circuit from the other parts of this circuit, and to avoid the undesirable influence from leakage currents. It is sufficient to insert this circuit only once in every three or four unit circuits. When the connective circuit is constructed in this way, the voltage which is across to each conductive transistor does not vary widely with the change of the length $h$, and it becomes possible to obtain constant pulse output.

If the value of the source voltage necessary for the largest $h$ is determined, the (absolute) maximum value of $E_k$ that is across the transistor $T(C_1)$ when the longest open connective circuit is formed shows little difference between the case when this circuit is inserted and the case when the source voltage $E$ becomes large. The maximum value of $E_k$ across $T(C_\nu)$, however, increases with the decrease of $\nu$ like stairs. Accordingly, only a few transistors with small $\nu$ are liable to be destroyed by supplying large voltage to them. Therefore, the problem can be avoided either by the use of the transistors with high maximum voltage ratings, or by the series connection of two transistors for such gates.

(2) *The Junction Circuit with Transformers*

Let us assume that the circuit $\Phi$ is constructed by the cascade connection of forty unit circuits. By cutting the connection at its center, namely between the 20 th and the 21 st unit circuits, and inserting a pulse transformer, we obtain the circuit under the consideration. Fig. 6 illustrates the junction part of $\Phi$. When the connective circuit has been extended to $T(S_{21})$, the pulse input drives $T_c$, and the circuit will be further extended to the right. When the open

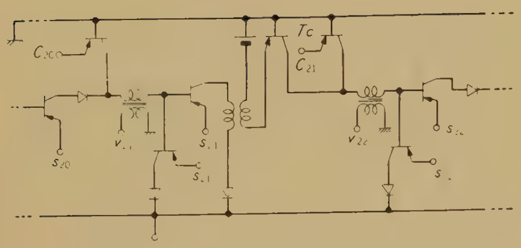


**Fig. 6**—The junction part of $\Phi$.

connective circuit reaches $T(S_{21})$, it is arranged by means of added emitter bias voltage that the leakage currents may not drive $T_c$. In order to keep the phase shift between the input and output currents of $T_c$ at a minimum, a transistor with a high $\alpha$ cutoff frequency should be used for $T_c$. Such a junction circuit serves to decrease to half the minimum value of $E_k$ across $T(C_1)$, as well as to decrease the maximum value of the leakage currents.

(3) *The Prevention of Leakage Currents*

In order to prevent leakage currents through $T(C_\nu)$ and $T(S_\nu)$ when the open connective circuit is formed, it is effective to bias the transistors negatively. This is because the voltage $E_k$ given to the collector induces a small pulse voltage in the emitters of non-driven transistors and degrades their cutoff characteristics.

The leakage current that flows through $G(\overline{S}_\nu)$ consists mainly of current flowing through the capacity of diode $d_\nu$ and its back resistance current. The value of the leakage current is comparatively large.

If NPN type transistors are used for $T(\overline{S}_\nu)$, diode $d_\nu$ is not necessary. In that case the leakage current is mainly derived from the collector capacity of the transistor, and the influence of the back current becomes almost negligible.

In order to prevent the leakage current flowing through the capacity of each gate element, the following contrivance is effective: we drive the input terminals so as to form the open connective circuit ($k=40$) while $\Phi$ is not driven, charge the capacities of all the gate elements, and let $\Phi$ perform its next operation before the stored charges have been dischaged. This is to avoid the leakage effect caused by the charging currents. The charge stored in the capacity of $G(\overline{S}_\nu)$ improves its conductive characteristic when $\Phi$ is driven.

## 3. Experimental Results

(*1*) *Forty Bit Carry Propagatng Circuits*

The author constructed the propagating circuit necessary to perform the addition of two binary numbers of 40 bits by using the circuits illustrated in Fig. 3 (b) and Fig. 6, and measured the dynamic characteristics of its operation. The pulse corresponding to each of $C$, $S$, and $\overline{S}$ was applied to the output pulse transformers of transistor amplifiers, the inputs of which were controled by a manual knife switch.

The conditions of the operation were: input pulse width,

$\tau_1=1\mu$ sec; input pulse repetition frequency,
$f=250$ kc; supply voltage of $\Phi$,
$-E=-3$ V; input current corresponding to the logical value 1,
$I_1=17$ mA; input current corresponding to the logical value 0,
$I_0 \doteqdot 0$; voltage given to the condenser K while $\Phi$ is not driven,
$e_k=-3$ V; voltage supply circuit-12 units output load resistance,
$R_L=100\,\Omega$; turns ratio of the output transformer, 1 : 3; junction circuit with transformer inserted (inserted at the 20th bit);
cutoff frequency of transistors used:
$f_\alpha=\left.\begin{matrix}4\text{ Mc}\\12\text{ Mc}\end{matrix}\right\}$ junction type, 30 Mc) drift type,

A few examples of the measured values are given in the Table 2, and some of the waveforms are shown in the Fig. 7. These examples contain the worst cases of $S/N$ ratio.

When the load resistance of the driving amplifier, is $100\,\Omega$, its output waveform is indicated by $w_9$ of Fig. 7.

In Table 2, the values of $\overline{v_2}$, $\overline{v_{11}}$, ·········$\overline{v_{41}}$

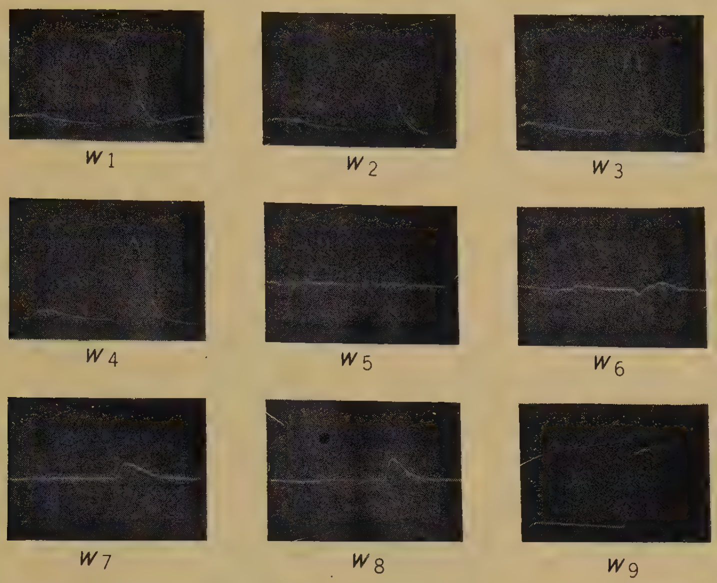


**Fig. 7**—Input and output waveforms.

**Table 2**

SOME EXAMPLES OF THE MEASURED VALUES AT 250 KC, 40 BITS. (V)

| Output Voltage / Case of Input | $\overline{v_2}$ | $\overline{v_{11}}$ | $\overline{v_{21}}$ | $\overline{v_{31}}$ | $\overline{v_{41}}$ | $\overline{v_{c1}}$ | $\overline{v_{c20}}$ |
|---|---|---|---|---|---|---|---|
| Closed Connective Circuit, *h* 40 (1 40) | 0. 45 | 0. 40 | 0. 32 | 0. 42 | 0. 35 | −10 | −7 |
| Waveform No. of Fig. 7 | $w_1$ | | $w_2$ | $w_3$ | $w_4$ | | |
| Open C.C. *k* 40 (1 40) | 0. 00 | 0. 01 | 0. 04 | 0. 07 | 0. 10 | −35 | −8 |
| Waveform No. of Fig. 7 | $w_5$ | | $w_6$ | $w_7$ | $w_8$ | | |
| Closed C.C. *h* 1 (1 2) | 0. 55 | | | | | | |

columns stand for the pulse voltages of the output terminals $v_2$, $v_{11}$, $\cdots\cdots\cdots v_{41}$ for various input cases. The values of $v_{c1}$ and $v_{c20}$ columns are DC collector voltages (values of direct currents) of $T(C_1)$ and $T(C_{20})$ respectively. (Their pulse amplitude is comparatively small.) In the "Case of Input" column, the values given to $h$ and $k$ indicate the length of closed or open connective circuits, and the contents in the parentheses designate the extent of the connective circuits, ranging from the beginning to the end bits.

If we define the SN ratio $\gamma_{SN}$ and the regulation of output pulse amplitude $\delta$ as follows, their values can be obtained from Table 2 as follows:

$$\gamma_{SN}=\frac{\text{Minimum output voltage in the longest}}{\text{Maximum output voltage in the longest}}$$

$$\times \frac{\text{value of } h}{\text{value of } k} = 3.2$$

$$\delta = \frac{\text{Maximum} - \text{Minimum}}{\text{Mean}} (\text{voltages in all}$$

$$\text{length of } h) = 50(\%).$$

Let us calculate the voltage $E_c$ which is across each transistor. If we calculate from the output values that the current which flows in the branch circuit is 11 mA for $h=20$ (i.e., when the junction of the transformer is at the 20th bit), and 18 mA for $h=1$, we can assume that the equivalent resistance of the diode is about 60Ω for $h=20$, and 50Ω for $h=1$; that the output load resistance reflected through each output transformer is about 10Ω; and that the voltage across capacitor $E_k$ is $-3$ V. Therefore, from Equation (5), $E_c=-0.3$ V for $h=20$, and $E_c=-1$ V for $h=1$. The latter corresponds to the case of $l_2$ in the Fig. 4, and the former to a proper line between $l_2$ and $l_3$. The ratio of collector current for the case $h=1$ to the case $h=20$ is about 2/3. This is in good accordance with the ratio of the output mean value for $h=1$ to that for $h=20$.

In the case of the open connective circuit, the voltage across the transistor of the first bit is calculated from Equation (6). If $e_0$ is taken not as the value in the Fig. 4 but as the experimental value (0.6–0.8 V), the calculated value $E_k$ will show a good agreement with the observed value ($-35$ V). Let us calculate the power dissipation of each conductive transistor for the case of $h=40$ (1∼40). From the current flowing into branch circuit 11 mA and the voltage across each transistor is about 3.3 mW, 0.3 V.

Using a low repetition frequency for driving the inputs, we can observe the increase of the leakage current through the capacity in each point. Accordingly charging action such as stated in 3.3 (iii) will be necessary.

No transistor was destroyed in the course of the present experiment. The performance of $\Phi$ was stable.

### (2) *The Carry Propagating Circuit That Corresponds to 20 Bits (A Half of the Whole Circuit Used Above)*

Experiments were performed on the half

**Table 3**

SOME EXAMPLES OF MEASURED VALUES AT 1 MC, 20 BITS (V)

| Output Voltages<br>Case of Input | $v_2$ | $v_6$ | $\bar{v}_7$ | $\bar{v}_{11}$ | $\bar{v}_{16}$ | $\bar{v}_{17}$ | $\bar{v}_{21}$ |
|---|---|---|---|---|---|---|---|
| $h=20$ (1∼20) | 0.75 | 0.70 | 0.70 | 0.65 | 0.55 | 0.55 | 0.70 |
| w.f. No. of Fig. 8 | $w_{13}$ | $w_{14}$ | | | $w_{15}$ | | $w_{16}$ |
| $k=20$ (1∼20) | 0.10 | 0.10 | 0.10 | 0.10 | 0.14 | 0.14 | 0.15 |
| w.f. No. of Fig. 8 | $w_{17}$ | $w_{18}$ | | | $w_{19}$ | | $w_{20}$ |
| $h=5$ (1∼5), $h=6$ (10∼15) | 0.70 | 0.50 | 0.10 | 0.18 | 0.55 | 0.15 | 0.10 |
| w.f. No. of Fig. 8 | $w_{21}$ | $w_{22}$ | $w_{23}$ | $w_{24}$ | $w_{25}$ | $w_{26}$ | $w_{27}$ |
| $h=5$ (1∼5), $k=11$ (10∼20) | 0.75 | 0.50 | 0.10 | 0.10 | 0.13 | 0.12 | 0.15 |
| w.f. No. of Fig. 8 | $w_{28}$ | $w_{29}$ | $w_{30}$ | $w_{31}$ | $w_{32}$ | | $w_{33}$ |

of the carry propagating circuit that was used in the above experiment (1). The present circuit excludes the junction circuit with transformers, and corresponds to 20 bits. The conditions of the experiments which were different from the former conditions are:

$$\tau_1 = 150\ \mathrm{m}\mu\mathrm{sec}, \quad f = 1\ \mathrm{Mc}, \quad I_1 = 28\ \mathrm{mA}$$

A few examples of the measured values are indicated in Table 3, and the waveforms are shown in Fig. 8. The upper part of $w_{10}$ in Fig. 8 is the input waveform which corresponds to $w_9$ in experiment (1). Only this part has a different voltage scale than the others. The lower part of $w_{10}$ is the same as $w_{10}$. Both of these waveforms display a phase shift between input and

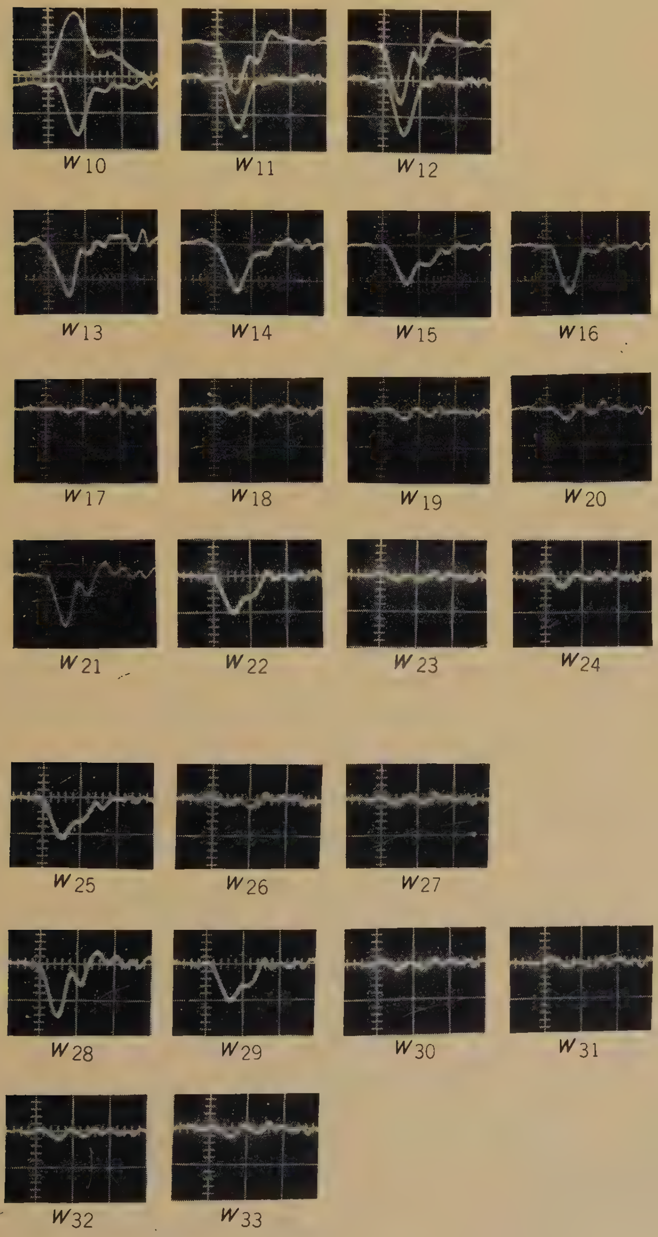

W10 W11 W12
W13 W14 W15 W16
W17 W18 W19 W20
W21 W22 W23 W24
W25 W26 W27
W28 W29 W30 W31
W32 W33

**Fig. 8**—Input and output waveforms.

output of about 20 m$\mu$ sec according to the observation. The upper and the lower parts of $w_{11}$ are the waveforms of the terminals $v_1$ and $v_{20}$ respectively, for $h_3$ (1~3) and $h_{15}$ (5~20). Likewise the two parts of $w_{12}$ are the waveforms of $v_1$ and $v_{20}$ respectively, for $h_{18}$ (1~18) and $h_2$ (19~20). These waveforms display a phase shift between the different output terminals, which was observed to be about 20 m$\mu$sec. From the measured values,

$$\gamma_{SN}=\frac{0.50}{0.15}=3.3$$

$$\partial=\frac{0.75-0.50}{0.625}=40(\%).$$

The ratio of the input current into the emitter to the current flowing in the connective circuit ranges from 55 to 80(%) in this case, whereas in experiment (1), the ratio ranges between 60 and 90(%). This is probably due to the decrease of $\alpha$ which is the current amplification factor of the transistor at the repetition frequency.

## 4. Application

### 4.1. Speeding up of Subtraction

For the subtraction of $(X-Y)$, the ordinary method is to add $X$ to the complement of 2 of $Y$. In order to get the complement of 2 of $Y$, however, we should use the negative value of each bit of $Y$, and 1 must be added in the binary way to the least significant bit of $Y$.

By making use of the $\Phi$ circuit, we can accomplish this addition of 1 simultaneouly with the performance of the functions of $\Phi$ described above. Namely, as is illustrated in Fig. 9, $\Phi$ is constructed by attaching the gate elements $G(C_0)$, $G(S_1)$, and $G(\overline{S_1})$ to the circuit of Fig. 3 (a). $G(S_1)$ and $G(\overline{S_1})$ are driven by the inputs corresponding to $S_1$ and $\overline{S_1}$.

It is arranged that $G(C_0)$ is driven only by the signal that assigns subtraction. This is accomplished by introducing the carry output signal to one bit before the least significant bit, in order to add 1. Therefore, in the case of subtraction, the value of $V_1$, obtained through $F_1$, is fixed as 1; and $Z_1$ is determined by $V_1$ and $S_1$. This is why no extra time is necessary to add 1.

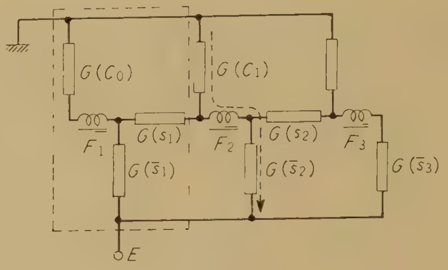


**Fig. 9**—$\Phi$ (The part necessary for subtraction).

### 4.2. Application to the Decimal Adder

The augend and the addend of decimal numbers of $n$ digits are indicated by

$$X=\sum_{\nu=1}^{n} X_\nu\cdot 10^{\nu-1},\quad Y=\sum_{\nu=1}^{n} Y_\nu\cdot 10^{\nu-1}$$

and the sum total by

$$U=\sum_{\nu=1}^{n+1} U_\nu\cdot 10^{\nu-1}.$$

Each of the digits $X_\nu$, $Y_\nu$, and $U_\nu$ can take integer values ranging from 0 to 9. These are coded into the excess three code using four binary bits as follows:

$$\left.\begin{aligned} X_\nu&=\xi_\nu(X_{\nu4}, X_{\nu3}, X_{\nu2}, X_{\nu1}) \\ Y_\nu&=\eta_\nu(Y_{\nu4}, Y_{\nu3}, Y_{\nu2}, Y_{\nu1}) \\ U_\nu&=\zeta_\nu(U_{\nu4}, U_{\nu3}, U_{\nu2}, U_{\nu1}) \end{aligned}\right\} \quad (7)$$

$X_{\nu\mu}$, $Y_{\nu\mu}$, and $U_{\nu\mu}$ ($\mu=4$, 3, 2, 1) are binary logical values. The addition of decimal numbers of one digit is denoted as follows:

$$X_\nu+Y_\nu=U_\nu \quad (8)$$

If this operation is executed through the use of the excess three code, the numerical relation is:

$$(X_\nu+3)+(Y_\nu+3)=(U_\nu+6) \qquad (9)$$

For $U_\nu \geq 10$, however, since the decimal carry output can be obtained, the values of the Equation (9) become larger than 15, and must be expressed by five bits.

Theretore, the value of the four bits excepting the fifth bit (carry output) is

$$(X_\nu+3)+(Y_\nu+3)=U_\nu+6-16=U_\nu-10. \quad (10)$$

If we pay attention to the four bits, these values are equal to the values of the Equation (9) when there is no decimal carry, and are equal to those of the Equation (10) when there is a decimal carry.

Therefore, in order to reduce these values to the correct excess three code, 3 should be subtracted in the case of Equation (9), and 3 should be added in the case of Equation (10). In other words, the above correction should be made according to whether $U_\nu \geq 10$ or not. When $U_\nu \geq 10$, the carry output is produced. Then a decimal number of $n$ digits can be regarded as a binary number of $4n$ bits, and two decimal numbers should be added in the binary way. Upon the results thus obtained, the above correction is made for each decimal digit, i.e., for each four binary digits. Then the decimal sum $U$, coded in the excess three code, can be obtained as the final result.

If the carry propagating circuit stated above is applied to such a binary method of addition, high speed addition becomes possible for decimal addition also. The block diagram of the decimal adder based on the

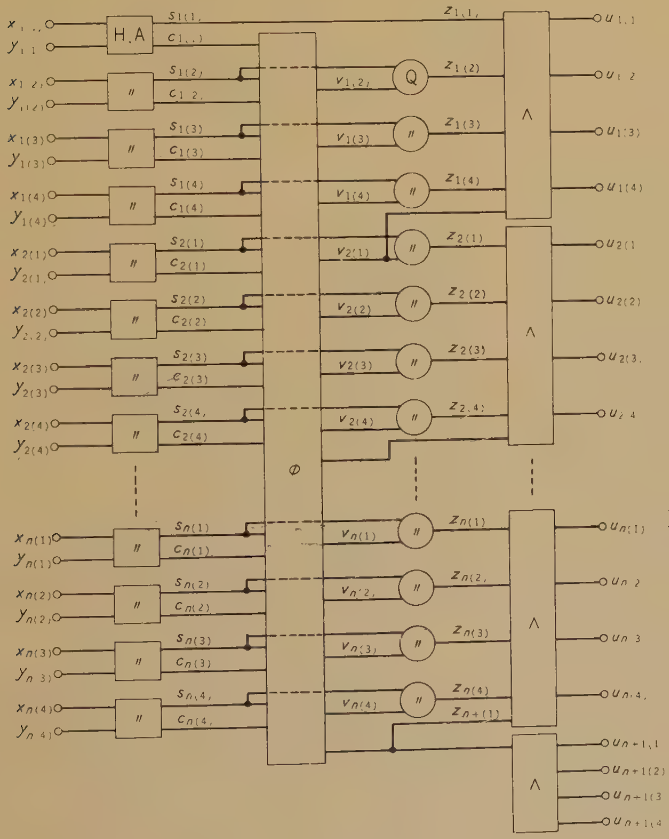


**Fig. 10**—Block diagram of parallel decimal adder.

**Table 4**

PROCESS OF DECIMAL ADDITION ($U=X+Y$)

| | 4 | 3 | 2 | 1 |
|---|---|---|---|---|
| $\mu$ | 4 3 2 1 | 4 3 2 1 | 4 3 2 1 | 4 3 2 1 |
| $X$ | 1 0 1 1 | 1 0 0 0 | 0 1 1 0 | 1 1 0 0 |
| $Y$ | 0 1 0 0 | 0 0 1 1 | 1 0 1 1 | 0 1 1 1 |
| $S$ | 1 1 1 1 | 1 0 1 1 | 1 1 0 1 | 1 0 1 1 |
| $C$ | 0 0 0 0 | 0 0 0 0 | 0 0 1 0 | 0 1 0 0 |
| $V$ | 0 0 0 0 | 0 1 1 1 | 1 1 1 1 | 1 0 0 0 |
| $Z$ | 1 1 1 1 | 1 1 0 0 | 0 0 1 0 | 0 0 1 1 |
| | (−) 1 1 | (−) 1 1 | (+) 1 1 | (+) 1 1 |
| $U$ | 1 1 0 0 | 1 0 0 1 | 0 1 0 1 | 0 1 1 0 |

$X$: 8539 $Y$: 1084 $U$: 9623

above principle is illustrated in Fig. 10, and the process of this addition is shown in Table 4.

The result of the binary addition of $X$ and $Y$ is indicated in the lower $Z$ line of Table 4. The resultant outputs are sent into the $Z$ terminals shown in Fig. 10. $\lambda$ is the symbol of the corrective action. Its function is to discern whether the $\nu$th the carry is obtained or not from the $(\nu+1)$th value of $V$, and to add (0 0 1 1) to the four bits of the same column, or subtract (0 0 1 1) from them. The function of $\lambda$ is performed in the corrective circuit $\Lambda$ shown in Fig. 10. The part of the circuit ranging from the input terminals to the $Z$ terminals in Fig. 10 is exactly the same as the circuit of Fig. 1.

## Conclusion

The carry propagating circuit $\Phi$, described in this paper, has the function of an adder. It is a completely new logical circuit, derived from an original concept.

If we regard $\Phi$ as a circuit of two dimensions made of $C$ and $S$, we shall be able to make circuits of many dimensions with ease. We shall also be able to construct logical circuit networks from the analogies of general geometrical models.

The author thinks that $\Phi$ can be an effective means for the construction of such current type logical circuits to realize special logical functions. He now expects that the logical function described as $V$ will be extracted from other switching circuits. He intends to improve the characteristics of $\Phi$ through change and reform and recognizes the need of researching about the storage effect of transistor in order to increase the repetition rating. He also welcomes readers' opinions and instructions. He is deeply grateful to Mr. T. Seki and Dr. T. Sakurai for their invaluable guidance and suggestions, and to Mr. T. Shina for his continuous cooperation in the experiments.

## References

(1) S. H. Caldwell, *Switching Circuit and Logical Design*, John Willey & Sons, Inc., New York (1958).

(2) R. K. Richard, *Digital Computer Component and Circuit*, D. Van Nostrand Co., Inc. (1957).

(3) A. Weinherger and J. L. Smith, "*A One-Microsecond Adder Using One-Megacycle Circuitry*," *IRE Trans. on Electronic Computers*, p. 65, June, 1956.

(4) H. Takahashi, "Calculating Machine II," in Iwanami Series, *Contemporary Applied Mathematics*, B 14 a II, Iwanami Shoten, Tokyo (In Japanese).

* * * *

681. 142:518. 5

# On the Generation of Prime Numbers using the Eratosthenes' Sieve by the MUSASINO-1*

**Katuhiko ARAI**†

*Generally it takes a very long time to generate prime numbers by means of iterated division with ordinary digital computers, for in them the speed of the division instruction is very slow compared to the speed of other instructions. In order to reduce the computing time, the writer composed a program utilizing the Eratosthenes' sieve. In this program the first difficulty is how to store the list of integers in the memory of the computer. This difficulty was solved by letting each binary digit of the memory represent one number of a list of ordinal numbers. The sieving process was programmed as follows: initially all the binary digits of the memory corresponding to the list are set to 1, and after all the bits that correspond to the compound numbers in the list are crossed out, an integer is found to be a prime number or not according to whether the corresponding bit is 1 or not.*

*First the writer composed a program to generate prime numbers smaller than 13,601. This reduced the computing time from one-fourth to one-third of that for the method of iterated division. Then he managed to generate prime numbers larger than a given $n_0$, using the above results. This reduced the time to less than one-tenth of the former time. The limit of the prime numbers obtainable by this method is $2^{38}$.*

## Introduction

Many programs to compute prime numbers with electronic computers have been composed, but as far as we know, most of them find prime numbers by iterated division. In other words, they generate prime numbers through the decision rule that an integer $n$ is prime if $n$ is not divisible by any prime number smaller than $\sqrt{n}$. In ordinary computers, the speed of division is very slow in comparison with that of other operations; therefore it always takes a very long time to generate prime numbers.

In order to reduce the time required for computation, we have discarded the method of iterated division and adopted that of the Eratosthenes' sieve. We have found that the latter method is much more effective than the former method, in reducing the computing time. Moreover, it seems that the same considerations that have been given to this method are applicable to various other programs.

## 1. The Program for Obtaining Prime Numbers Smaller than 13,601

In making a program to generate prime numbers by the Eratosthenes' sieve, the first difficulty is how to store the list of integers in the memory of the computer. In an ordinary program of numerical calculations, the numerical value of a number is stored as a word in the memory of the computer. However, in such a method, there are so many wasted bits, and the memory capacity of the computer is so small, that it is almost impossible to carry out sieving program with the computer. If we use the Eratosthenes' sieve, however, we need not know the numerical values of each integer in the process of the operation. What we need to know is only the order of the integers in the list. Their numerical values are necessary only when it comes time to print them.

---

* This research has been conducted while the writer was receiving training in the Electronics Research Section. The original MS was received by the E.C.L., on Dec. 7, 1959 and published in the *Electrical Communication Laboratory Technical Journal*, N.T.T., Vol. 9, No. 2, 1960.

† Administration Section, Administration Division.

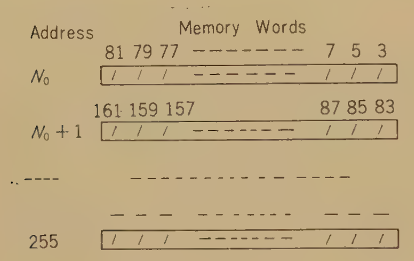
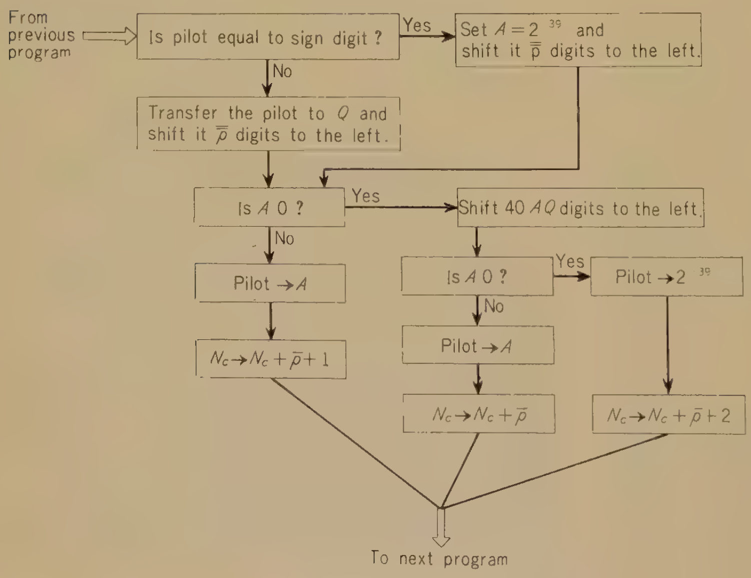


**Fig. 1**—The way of attaching numbers. (The left end digit is the sign digit.)

Now we assume that each integer is represented by one binary digit of the memory of a binary digital computer such as the MUSASINO-1. Since the prime numbers larger than 2 are all odd, we only represent the odd ordinals, from 3 up, by the bits of memory as illustrated in Fig. 1. At first, we set all the bits of memory to 1, and cross out bits corresponding to multiples one after another. After the sieving process is over, we can decide whether an integer is prime or not according to whether the corresponding bit is 1 or 0.

Next let us consider how to decide whether the bit of an integer $n$ is 0 or 1. We compose a word in which the bit of $n$ is 1 and all the other 39 digits are 0, and call this word the pilot of $n$. If we operate the logical product of this pilot and the address in which $n$ is situated, we can determine whether the digit is 0 or 1 according to whether the result is 0 or not. When we want to cross out a digit, we only have to operate the logical product of the pilot and the considering address, and further the modulo 2 sum of this result and the address.

From Fig. 1 it is known that shifting one digital position to the left corresponds to adding 2 to the number represented by the digits of the memory. When we cross out the bit of $n=rp$, the next bit to be crossed out is that of $(r+2)p=n+2p$. Therefore the bit of $n+2p$ is the $p$th bit from that of $n$ to the left. From the way of representing numbers illustrated in Fig. 1, we can easily find that we have to increase the number of


From previous program
Is pilot equal to sign digit ?
Yes
Set $A=2^{39}$ and shift it $\bar{p}$ digits to the left.
No
Transfer the pilot to $Q$ and shift it $\bar{\bar{p}}$ digits to the left.
Is $A$ 0 ?
Yes
Shift 40 $AQ$ digits to the left.
No
Pilot →$A$
$N_c \to N_c+\bar{p}+1$
Is $A$ 0 ?
Yes
Pilot →$2^{39}$
No
Pilot →$A$
$N_c \to N_c+\bar{p}$
$N_c \to N_c+\bar{p}+2$
To next program

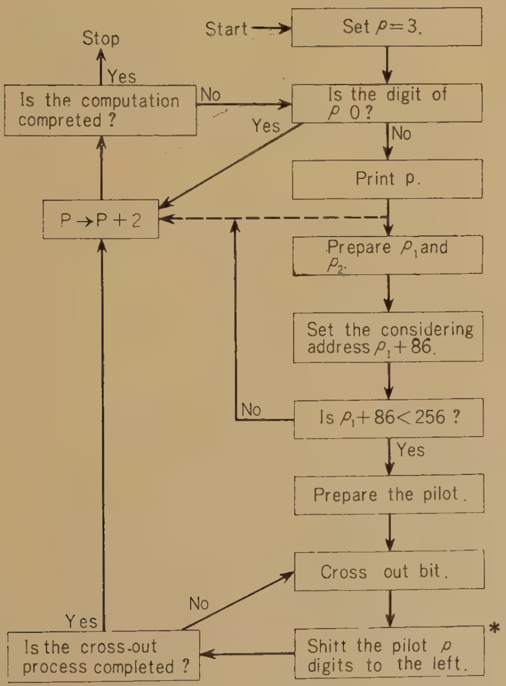
Notations:
$\bar{p}$, $\bar{\bar{p}}$: $p=40\bar{p}+\bar{\bar{p}}+1$, where $2 \leq \bar{\bar{p}} \leq 40$.
$a \to b$: substitute $b$ for $a$.
$N_c$: the address in which a bit should be crossed out.

**Fig. 2**—The flow-chart to appoint next multiples.

the address when the shifted pilot overflows. This can be done according to the process shown in the flow chart of Fig. 2.

When we cross out the multiples of $p$, we may begin the process from $p^2$, since the multiples smaller than $p^2$ have been crossed out as the multiples of the prime numbers smaller than $p$. The position of the bit of $p^2$ is the $\{(p_2/2)+1\}$th place from the right end of the address $N_0+p_1$, where $p_1$ and $p_2$ are the quotient and remainder of $(p^2-3)/80$, respectively. This is to say that the address from which we ought to begin the crossing-out process is $N_0+p_1$, and the initial pilot is obtained by shifting the right end bit $p_2/2$ digital positions to the left.

From the above considerations, we obtain the flow chart shown in Fig. 3. Our program is composed of 85 words. Since the memory capacity of the MUSASINO-1 is 256 words and one word consists of 40 bits, we can obtain prime numbers smaller than 13,601 by this program.



Notations:
$p_1$, $p_2$: $p^2=80p_1+3+p_2$, where $0\leq p_2<80$.

**Fig. 3**—The flow-chart to compute prime numbers smaller than 13,601.

## 2. The Program to Obtain Prime Numbers Larger than a Given Integer $n_0$

By the program explained above, we obtain the prime numbers from 3 to 13,597. By using these results, we can further obtain the prime numbers smaller than 184,878,409 ($=13{,}597^2$). Next we make a program to obtain prime numbers larger than a given integer $n_0$ by means of the Eratosthenes' sieve.

Here the prime numbers obtained above are punched in a tape, and they are read in the computer one by one, while their corresponding multiples in the stored list are sieved out. In the previous program, we first set all the bits of the addresses, ranging from $n_0$ to 255, to 1, as the list of odd integers. In the present program, however, we set them all to 0 at first and then store 1 in the digits corresponding to the multiples of the prime numbers that have been read in. Therefore the decision rule is reverse from the previout one; namely, if a digit is 1, the corresponding integer is not prime, and if it is 0, it is prime. As a result, we need only operate the logical sum to store 1 in the corresponding bit in this program, whereas in the previous one we had to operate two logical operations; i.e., the logical product and the modulo 2 sum.

Next, let us consider how to indicate the position of $p$'s smallest odd multiple larger than $n_0$. If $p^2>n_0$, there is no difficulty because we can apply the same operation to $p^2-n$ as we did on $p^2-3$ in the above section. Therefore we consider the case only when $p^2<n$. Let $q$ and $r$ be the quotient and remainder of $n_0/p$ respectively, and we find the following facts: if $r$ is even, $p$'s smallest odd multiple in the list is $n_0+2p-r$, occupying the $(p-r/2)$th digital position from that of $n_0$ to the left; and if $r$ is odd, the multiple is $n_0+p-r$, occupying

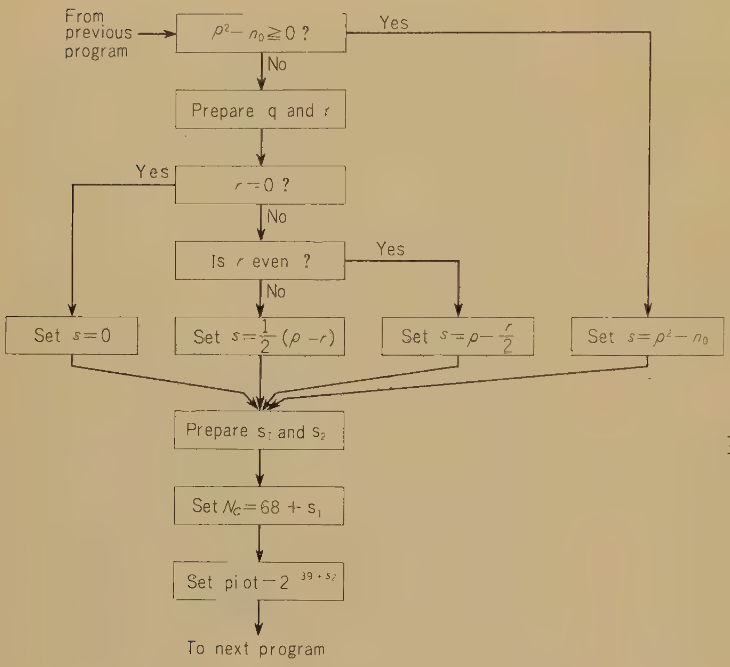
---

* The detail of this part is shown in Fig. 2.

the $(p-r)/2$th digital position from that of $n_0$ to the left. When $(p-r/2)$ or $(p-r)/2 > 40$, we need the same consideration as we gave to preparing pilots in the previous section.

From these considerations, we can obtain the flow chart that designates the address and the bit from which to begin the sieving process. This flow chart is given in Fig. 4.

The flow chart of the whole program is illustrated in Fig. 5. By this program, we can obtain the list of prime numbers in the



Notations:

$q$, $r$: $n=pq+r$, where $0 \leqq r < 40$.

$$s:\ s=\begin{cases} p^2-n_0 & (p^2>n_0),\\ (p-r)/2 & (p^2<n_0,\ r\text{: odd}),\\ (2p-r)/2 & (p^2<n_0\ r\text{: even}).\end{cases}$$

$s^1$, $s_2$: $s=40s_1+s_2$ where $0 \leqq s_2 < 40$.

**Fig. 4**—The flow-chart that appoints the address and the bit from which to begin the sieve process.

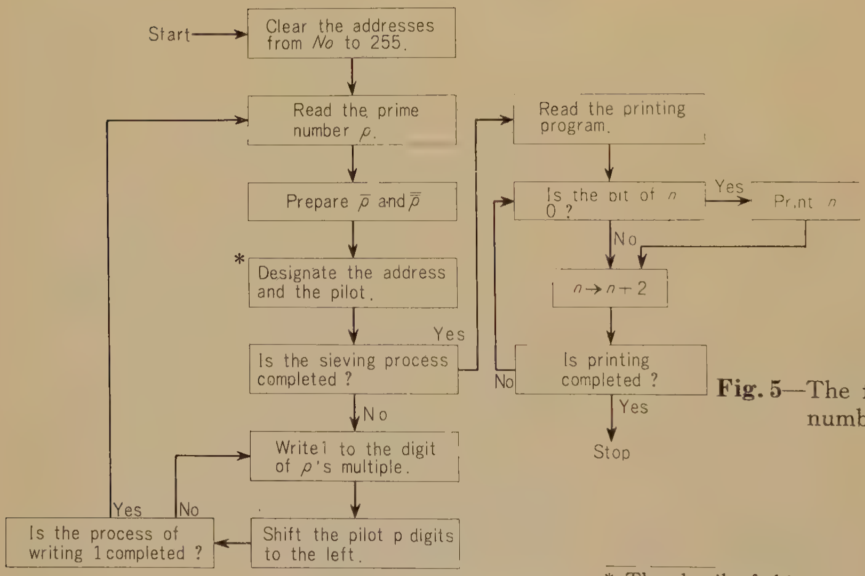

Start
Clear the addresses from $N_0$ to 255.
Read the prime number $p$.
Prepare $\bar{p}$ and $\bar{p}$
*
Designate the address and the pilot.
Yes
Is the sieving process completed ?
No
Write 1 to the digit of $p$'s multiple.
Shift the pilot p digits to the left.
Is the process of writing 1 completed ?
Yes
No
Read the printing program.
Is the bit of $n$ 0 ?
Yes
Print $n$
No
$n \rightarrow n+2$
Is printing completed ?
No
Yes
Stop

**Fig. 5**—The flow-chart to obtain prime numbers larger than $n_0$.

---

* The detail of this part is shown in Fig. 4.

range from the given $n_0$ to $n_0+15{,}040$, where $n_0+15{,}040<2^{38}$. The necessary data are the prime numbers smaller than $\sqrt{n_0+15,040}$ excepting 2.

### Conclusion

A program has been composed to obtain prime numbers by means of iterated division in our laboratory. Compared with the results of this program, the method proposed here is remarkably effective in reducing computing time. The latter takes only about one-third to one-fourth of the time needed for the former method when the numbers under consideration are relatively small, and when they are large, it takes only one tenth or less time. This is because the speed of the division instruction is extremely slow compared with that of other instructions.

In the method of iterated division, we have to store the prime numbers smaller $\sqrt{N}$ in the computer in order to get the prime numbers up to $N$. Therefore the upper limit of obtainable prime numbers is restricted by the memory capacity of the computer. However, in the present method, there is an advantage of having no such restriction, for we only have to store the prime numbers smaller than $\sqrt{N}$ in a tape.

* * * *

# Papers Contributed to Scientific and Technical Journals by the Members of the Laboratory*

## Papers Published in Other Publications of the Elecirical Communication Laboratory

**U.D.C. 62.001:620.2**

Research, Development, and Design
*Toshio HAYASAKA*
Kenkyû Zituyôka Hôkoku (Electr. Comm. Labor. Techn. Journ.), NTT, **9**, 1, pp. 1–27, Jan. 1960.

**U.D.C. 621.316.5.021.001.2:(620.17:658.516)**

Technical Study on Weak-Current Contact Materials
*Kinya TUTIYA*
Kenkyû Zituyôka Hôkoku (Electr. Comm. Labor. Techn. Journ.), NTT, **9**, 2, pp. 135–182, 1960

The author established the standard test method and also increased the performance of weak current contact materials. This study also led to an increased understanding of the factors which cause variations in the measured values. (in Japanese)

**U.D.C. 621.318.56:921.394.6]:620.178**

Deterioration of Contacts of a Polar Relay with a Rigid Tongue
*Sanae AMADA*, *Kosaku MUKAI*, and *Yukichi KANEKO*
Kenkyû Zituyôka Hôkoku (Electr. Comm. Labor. Techn. Journ.), NTT, 9, 1, pp. 64–82, Jan. 1960

As a result of deterioration tests of polar relay contacts, many unexpected weldings were observed. Molybdenum contacts and spark quench circuits having resistances larger than three hundred ohms were used to prevent weldings. (in Japanese)

**U.D.C. 621.391.833:621.376.56**

Transmission Performance of Code Modulation Systems
*Yukio HOSHIKO*, *Kazuo KIMURA*, and *Takao ARAKI*
Kenkyû Zituyôka Hôkoku (Electr. Comm. Labor. Techn. Journ.), NTT, **9**, 2, pp. 83–118, 1960

Transmission performance of code modulation systems, P.C.M. and Delta Modulation, is analyzed. Especially, the noise characteristics of the coding and the repeating parts are calculated. (in Japanese)

**U.D.C. 621.395.31.001.2(083.5)**

Tables of Telephone Traffic Formulae No. 1—Table for Waiting System with Full Availability (Infinite Sources)*
*Terunobu SUZUKI*
Kenkyû Zituyôka Hôkoky (Electr. Comm. Labor. Techn. Journ.), NTT, 3rd Extra Issue, Nov. 1959

---

* Reprints may be available upon your request to the author.

The waiting formulae of telephone traffic theory have been hitherto used mainly for estimating the numbers of trunks and operators required for manual telephone exchanges. However, with the advance of common control automatic telephone exchange systems, the formulae are not only used for the above calculations, but also largely as a basis for planning the grouping of common control equipments and in estimating their required numbers, despite of their importance, no sufficiently comprehensive and accurate tables of this kind seem to exist in print; therefore we thought it would be useful to publish the results of some tabulations.

This table is usable for a waiting system with full availability on the assumption of a Poisson distribution of calls, negative exponential holding times, and an infinite number of sources. The table comprises probabilities of waiting and average waiting times for different traffic values and defferent numbers of trunks which have been calculated from the waiting formulae that are well-known as Englang's C formula.

The calculated results are expressed with an accuracy of eight decimal places. The traffic values contained in the table are given for the following intervals in the following ranges:

| Interval | Range |
|---|---|
| 0. 001 | 0. 001– 0. 080 |
| 0. 002 | 0. 080– 0. 200 |
| 0. 005 | 0. 200– 0. 400 |
| 0. 01 | 0. 40 – 0. 80 |
| 0. 02 | 0. 80 – 2. 00 |
| 0. 05 | 2. 00 – 8. 00 |
| 0. 1 | 8. 0 – 20. 0 |
| 0. 2 | 20. 0 – 40. 0 |
| 1. 0 | 40. 0 –100 |

The numbers of trunks are given by integers larger than the traffic values and are limited within the range where the avarage waiting time can exceed the avarage holding time $\times 10^{-6}$.

For the convenience of comparison with the probabilities of waiting, Erlang's loss probabilities are also given; because they were obtained during the course of the calculation of above waiting probabilities.

The calculation has been carried out on the MUSASINO-1 electronic digital computer constructed in the Electrical Communication Laboratory, NTT, Japan. This table is the first of a projected series of tables of traffic formulae required in the design of telephone plants.

0. 85

| | | | | |
|---|---|---|---|---|
| 1 | 0. 85000000 | 0. 45945946 | 0. 85000000 | 5. 66666667 |
| 2 | 0. 42500000 | 0. 16336913 | 0. 25350877 | 0. 22044241 |
| 3 | 0. 28333333 | 0. 04424014 | 0. 06066930 | 0. 02821828 |
| 4 | 0. 21250000 | 0. 00931347 | 0. 01179698 | 0. 00374507 |
| 5 | 0. 17000000 | 0. 00158079 | 0. 00190395 | 0. 00045878 |
| 6 | 0. 14166667 | 0. 00022389 | 0. 00026084 | 0. 00005060 |
| 7 | 0. 12142857 | 0. 00002719 | 0. 00003094 | 0. 00000503 |
| 8 | 0. 10625000 | 0. 00000289 | 0. 00000323 | 0. 00000045 |

0. 95

| | | | | |
|---|---|---|---|---|
| 2 | 0. 47500000 | 0. 18792296 | 0. 30593220 | 0. 29136400 |
| 3 | 0. 31666667 | 0. 05616653 | 0. 08010979 | 0. 03907794 |
| 4 | 0. 23750000 | 0. 01316395 | 0. 01719370 | 0. 00563728 |
| 5 | 0. 19000000 | 0. 00249491 | 0. 00307833 | 0. 00076008 |
| 6 | 0. 15833333 | 0. 00039487 | 0. 00046912 | 0. 00009289 |
| 7 | 0. 13571429 | 0. 00005397 | 0. 00006200 | 0. 00001025 |
| 8 | 0. 11875000 | 0. 00000636 | 0. 00000722 | 0. 00000102 |
| 9 | 0. 10555555 | 0. 00000067 | 0. 00000075 | 0. 00000009 |

**U.D.C. 621.395.61/.062.001.2:621.391.883**

### Design Requirements of a Telephone Set from the Standpoint of Transmission Quality

*Zenzi YAMAGUCHI*

Kenkyû Zituyôka Hôkoku (Electr. Comm. Labor. Techn. Journ.), NTT, **9**, 1, pp. 28–63, Jän. 1960

In a design of a new telephone set consideration is given to the problem of what characteristics are most desirable for a telephone set from the point of view of transmission quality. (in Japanese)

**U.D.C. 621.396.65.029.64:621**

Research on 24 channels P.C.M. Terminal Equipment
*Kohichi YAMAGUCHI*
Kenkyû Zituyôka Hôkoku (Electr. Comm. Labor. Techn. Journ.), NTT, **9**, 2, pp. 119–134

Odd and even group channels are coded separately by 7 bit gray coded tube. Simplified separation circuit and high speed coding and decoding devices characterize the 24 channels P.C.M. Terminal Equipment. (in Japanese)

**U.D.C. 681.142:518.5**

On the Generation of Prime Numbers by the Sieve of Eratosthenes using MUSASINO-1
*Katsuhiko ARAI*
Kenkyû Zituyôka Hôkoku (Electr. Comm. Labor. Techn. Journ.), NTT, **9**, 2, pp. 183–195, 1960

A program for generating prime numbers by the Sieve of Eratosthenes was made. It sieves compound numbers from tbe sequence of odd integers represented by each bit of the memory. (in Japanese)

## Papers Published in Publications of Scientific and Technical Societies

**U.D.C. 621.391.833.43**

Distortion Distribution and Error Probability in Binary Transmission System
*Yukio HOSHIKO*, *Tosi MINAMI*, and *Takasi OMORI*
Journ. Inst. Electr. Comm. Engrs. Japan, **43**, 2, pp. 146–153, Nov. 1960

In this report we discussed the residual response and analyzed the general form of the distribution function of the residual response in a binary transmission system. Also, we analyzed the relation between the error rate and the distribution function of the residual response. (in Japanese)

**U.D.C. 678.742:541.64**

Second Order Transition of Polyethylene
*Ryuichi NAKANE*
Journ. Appl. Polym. Science, **3**, Issue 7, pp. 124–125 Jan.-Feb., 1960

Among the phenomena which were hitherto treated as the second order transition of polyethylene there exist at least two different phenomena: the end point of crystallinity change at $-30°$ C, and the true second order transition at $-55°$ C.

**U.D.C. 681.142**

High Speed Shifting Circuit
*Noriyoshi KUROYANAGI*
Journ. Inst. Electr. Comm. Engrs. Japan, **43**, 2. pp. 188–193, Feb. 1960

This circuit, made of several transistor gates and several pulse transformer voltage feeders, can shift the number entered into this circuit in one step as *n* figures, but has no storage faculty. (in Japanese)

**U.D.C. 681.18:621.374.3**

Address-Selection System for Two-Alternating Current Memory System
*Shigeharu YAMADA* and *Teruhiko BESSHO*
Journ. Inst. Electr. Comm. Engrs. Japan, 43, 2, pp. 193–199, Feb. 1960

An address-selection system which makes use of the combination of a linear selection circuit (utilizing error correcting codes) and diode amplitude filters is described. Each filter is constructed by the parallel connection of a linear transformer, two diodes connected oppositely in series, and a load. The selection ratio is improved by the use of filters. (in Japanese)

* * * *

# CONTENTS

A Computer Program to Find Boolean Functions Representable by a Single Logical Element Based on a Majority Decision Principle ............ 89
*Saburo MUROGB*

Measurement of Thermal Conductivity in Semiconductors ........................ 99
*Riro NII*

Semiconductor Speech-Path Switches Suitable for Direct-Coupled Connection ........................................... 105
*Ichiro ENDO* and *Shoji YOSHIDA*

The Nonlinear Barrier Capacitance of Silver Bonded Diodes ........................ 112
*Shoichi KITA* and *Roichi SUGIYAMA*

VHF Crystal Polishing and the Nature of Polished Quartz Surfaces .............. 119
*Ichiro IDA and Yuzo ARAI*

High Speed Adding System ................................................ 175
*Noriyosi KUROYANAGI*

On the Generation of Prime Numbers using the Eratosthenes' Sieve by the MUSASINO-1 ................................ 189
*Katuhiko ARAI*

Papers Contributed to Scientific and Technical Journals by the Members of the Laboratory ........................................ 194

*Copyright 1960 by the Electrical Communication Laboratory, NTT*